

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG/Memory	3,4 5,6 7
CPU-Power ,CPU-GND	8,9
DDRIV X8	10,11,12,13,14,15
PCH-LPC/HDA/RTC/MISC/SPI	16
PCH-DMI/PCIE/USB/SATA	17
PCH-CLK/GPIO	18
PCH-POWER/GND	19,20
PCH Strap	21
Dual BIOS	22
PCIESLOT	23,24,25
SIO-NTC6779D/PS2	26
FAN CONTROLLOR-1	27,28
CLK GEN4105	29
ALC892/887	30
LAN RTL8111G/8106E	31
USB3.0-VL805	32,33
SATA Connector	34
Rear/Front USB2.0/USB3 Connector	35,36
ACPI Controller UPI	37
CPU Power-ISL6388	38
CPU Power -ISL6611	39
CPU Power -MOS	40,41
DDR Power	42,43,44
PCH Power	45,46
ATX F_Panel/EMI /TPM	47
XDP / Manual Parts	48

MS-7882

Haswell-E Platform

ATX

Ver: 1.0

CPU:

Haswell-E

System Chipset:

Wellsburg

Onboard Chip:

HD Audio Codec: ALC1150

LAN-Killer LAN

SIO:NTC6792D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

DDRIV (1666MHz) * 8 (Dual Channel)

ACPI:

ISL6388

PWM:

VRD12.5 -ISL6388

Expansion Slots:

PCI Express (X16) Slot1

PCI Express (X8) Slot2

PCI Express (X8) Slot3

PCI Express (X16) Slot4

PCI Express (X8) Slot5

Other:

SATA3.0 *8

USB2.0 *8

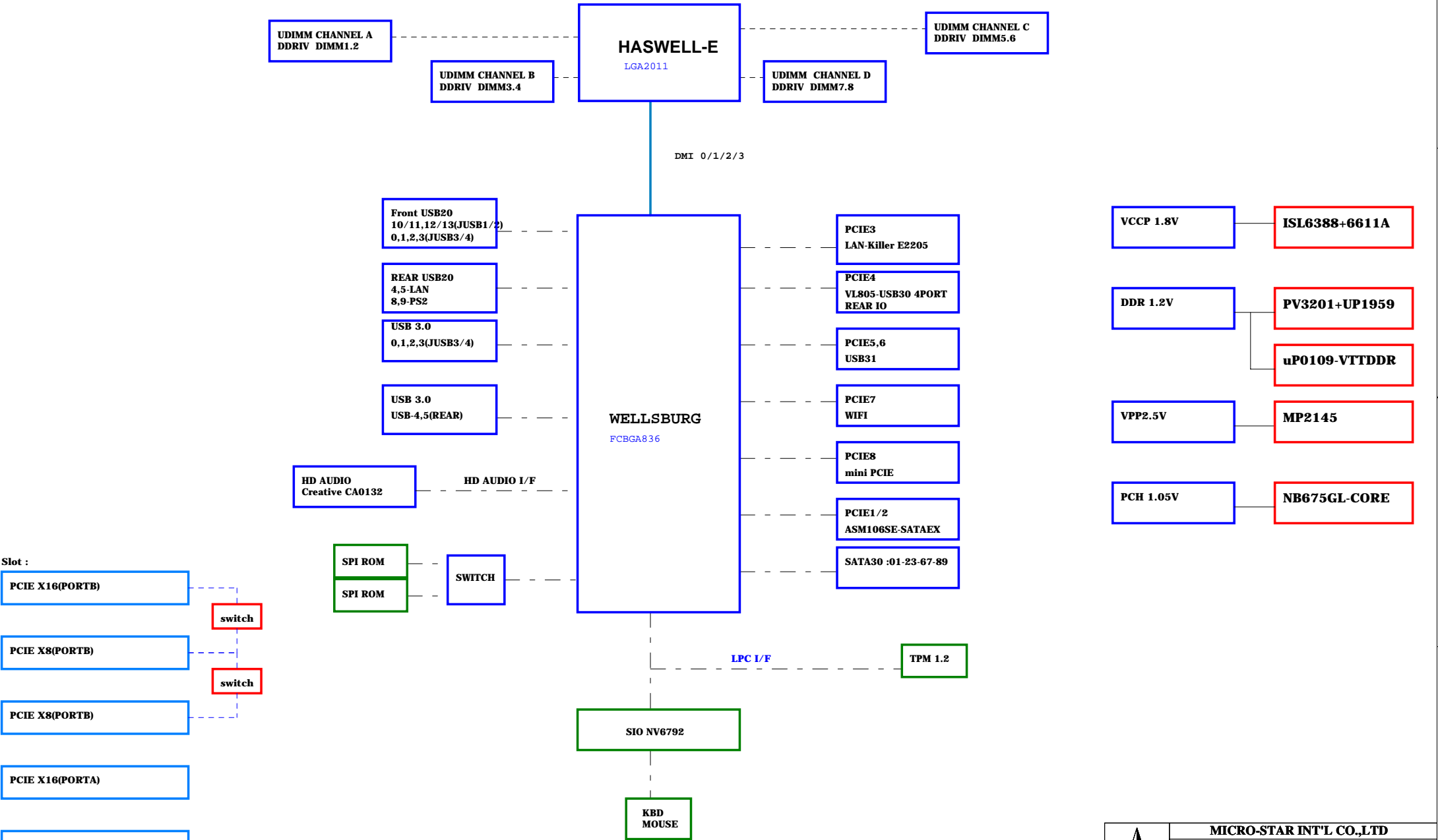
USB3.1 *1

REAL USB3.0 *6

FRONT USB2.0 *4

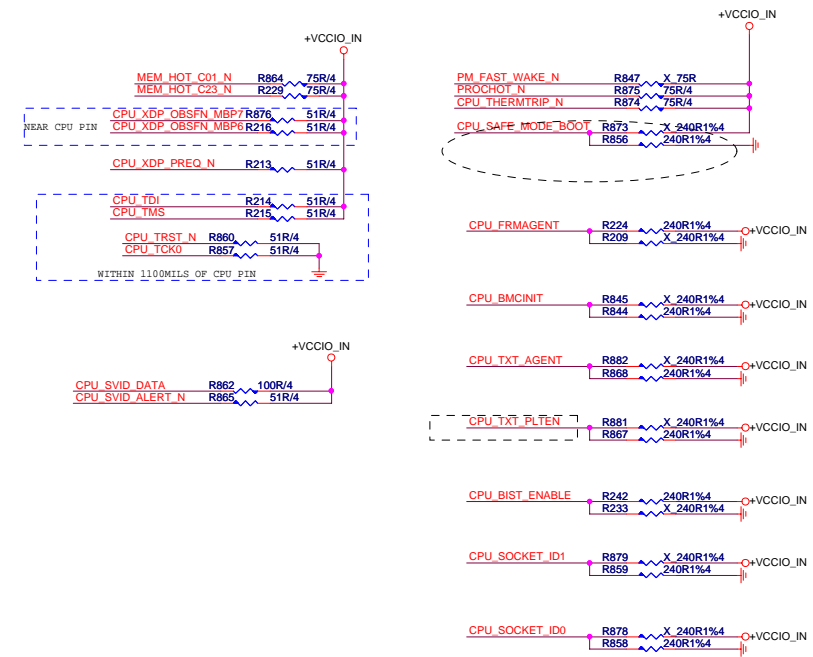
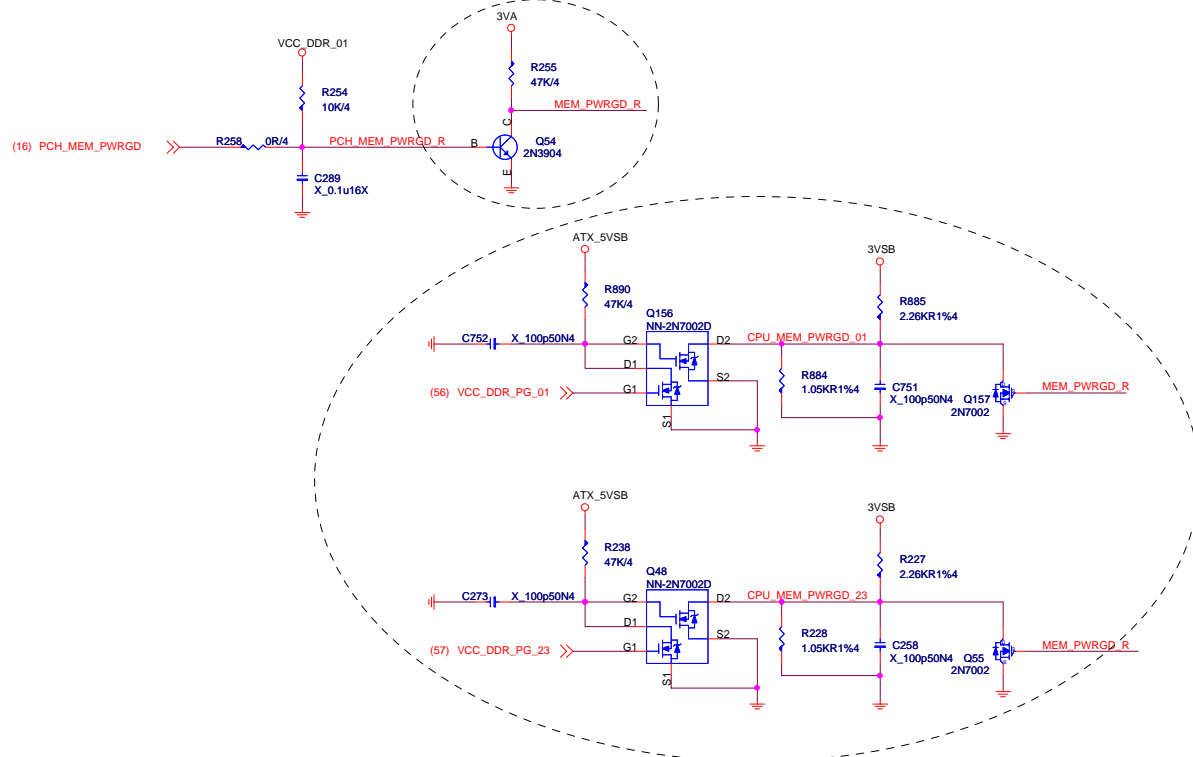
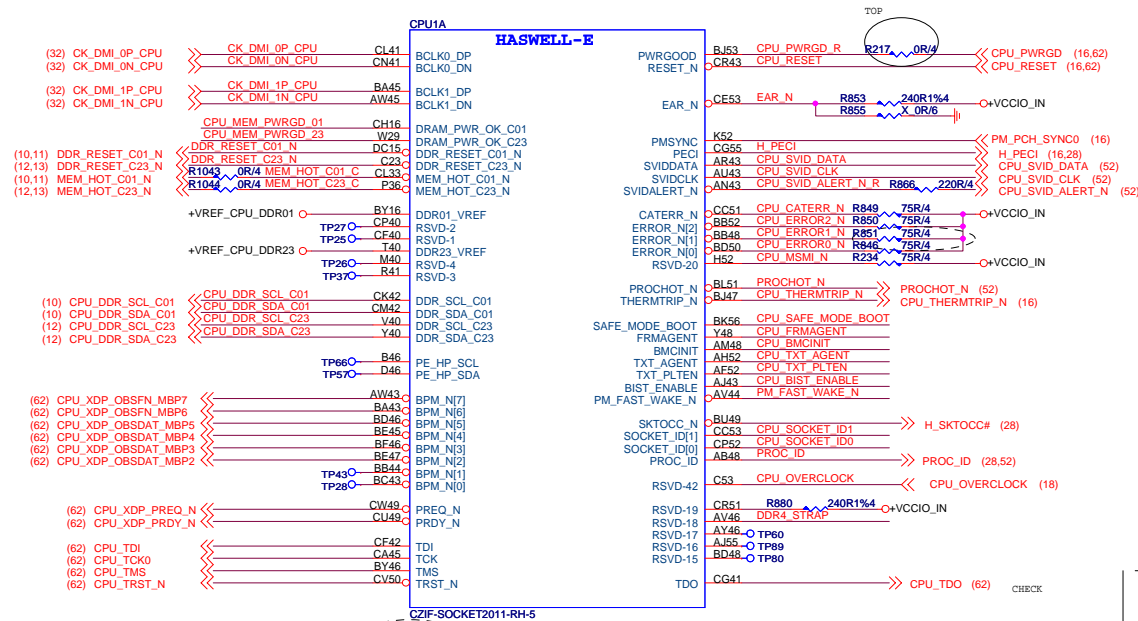
FRONT USB3.0 *4

MS-7882 Block Diagram



CPU-CLK/Control/MISC

OR:R278 REMOVED



Slow mode circuit

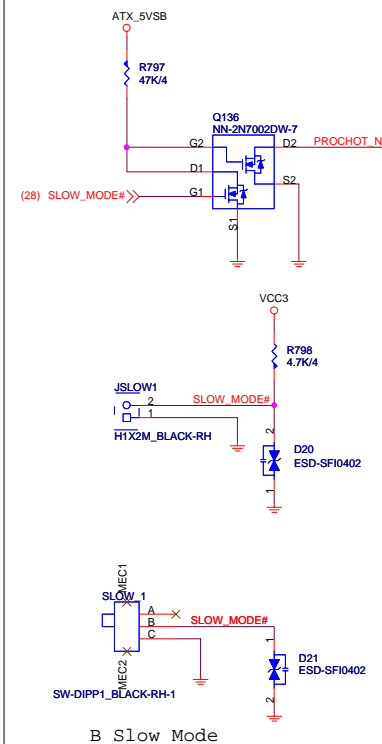


Figure 10 shows the schematic of the CPU and memory bus connections. It includes four signal lines, each with a resistor connected to a VCCIO_IN pin:

- CPU_OVERCLOCK:** Connected to VCCIO_IN via resistor R235 (10K/4). A label R237 X 0R/6 is also present.
- DDR4_STRAP:** Connected to VCCIO_IN via resistor R852 (10K/4). A label R854 X 0R/6 is also present.
- H_SKT0CC#:** Connected to VCCIO_IN via resistor R877 (10K/4).
- PROC_ID:** Connected to VCCIO_IN via resistor R210 (10K/4).

All VCCIO_IN pins are connected to a common VCC3 pin.

PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V



MICRO-STAR INT'L CO.,LTD

MS-7882

Size Custom	Document Description CPU-CLK/Control/MISC	Rev 1.0
Date: Thursday, June 26, 2014		Sheet 3 of 66

CPU-DMI / PEG

CPU1F

HASWELL-E

(17) DMI_RX3	DMI_RX3	C248	0.1u/10X4 DMI CPU RX3	E47	DMI_RX_DP[3]	D42	DMI CPU TX3	C252	0.1u/10X4 DMI TX3	>>DMI_TX3 (17)
(17) DMI_RX2	DMI_RX2	C265	0.1u/10X4 DMI CPU RX2	D48	DMI_RX_DP[2]	E43	DMI CPU TX2	C268	0.1u/10X4 DMI TX2	>>DMI_TX2 (17)
(17) DMI_RX1	DMI_RX1	C246	0.1u/10X4 DMI CPU RX1	E49	DMI_RX_DP[1]	D44	DMI CPU TX1	C259	0.1u/10X4 DMI TX1	>>DMI_TX1 (17)
(17) DMI_RX0	DMI_RX0	C263	0.1u/10X4 DMI CPU RX0	D50	DMI_RX_DP[0]	E45	DMI CPU TX0	C267	0.1u/10X4 DMI TX0	>>DMI_TX0 (17)
(17) DMI_RX3#	DMI_RX3#	C249	0.1u/10X4 DMI CPU RX3#	C47	DMI_RX_DN[3]	B42	DMI CPU TX3#	C253	0.1u/10X4 DMI TX3#	>>DMI_TX3# (17)
(17) DMI_RX2#	DMI_RX2#	C266	0.1u/10X4 DMI CPU RX2#	B48	DMI_RX_DN[2]	C43	DMI CPU TX2#	C270	0.1u/10X4 DMI TX2#	>>DMI_TX2# (17)
(17) DMI_RX1#	DMI_RX1#	C247	0.1u/10X4 DMI CPU RX1#	C49	DMI_RX_DN[1]	B44	DMI CPU TX1#	C251	0.1u/10X4 DMI TX1#	>>DMI_TX1# (17)
(17) DMI_RX0#	DMI_RX0#	C264	0.1u/10X4 DMI CPU RX0#	B50	DMI_RX_DN[0]	C45	DMI CPU TX0#	C268	0.1u/10X4 DMI TX0#	>>DMI_TX0# (17)
(47) EXP_C_RXP_7				M56	PE1B_RX_DP[7]	L49			>>EXP_C_TXP_7 (47)	
(47) EXP_C_RXP_6				L57	PE1B_RX_DP[6]	K48			>>EXP_C_TXP_6 (47)	
(47) EXP_C_RXP_5				M54	PE1B_RX_DP[5]	L47			>>EXP_C_TXP_5 (47)	
(47) EXP_C_RXP_4				L53	PE1B_RX_DP[4]	K46			>>EXP_C_TXP_4 (47)	
(47) EXP_C_RXN_7				K56	PE1B_RX_DN[7]	J49			>>EXP_C_TXN_7 (47)	
(47) EXP_C_RXN_6				J57	PE1B_RX_DN[6]	H48			>>EXP_C_TXN_6 (47)	
(47) EXP_C_RXN_5				K54	PE1B_RX_DN[5]	J47			>>EXP_C_TXN_5 (47)	
(47) EXP_C_RXN_4				J53	PE1B_RX_DN[4]	H46			>>EXP_C_TXN_4 (47)	
(27) EXP_C_RXP_3				G55	PE1A_RX_DP[3]	L45			>>EXP_C_TXP_3 (27)	
(27) EXP_C_RXP_2				F54	PE1A_RX_DP[2]	K44			>>EXP_C_TXP_2 (27)	
(27) EXP_C_RXP_1				F52	PE1A_RX_DP[1]	L43			>>EXP_C_TXP_1 (27)	
(27) EXP_C_RXP_0				F51	PE1A_RX_DP[0]	K42			>>EXP_C_TXP_0 (27)	
(27) EXP_C_RXN_3				E55	PE1A_RX_DN[3]	L45			>>EXP_C_TXN_3 (27)	
(27) EXP_C_RXN_2				D54	PE1A_RX_DN[2]	H44			>>EXP_C_TXN_2 (27)	
(27) EXP_C_RXN_1				D52	PE1A_RX_DN[1]	J43			>>EXP_C_TXN_1 (27)	
(27) EXP_C_RXN_0				C51	PE1A_RX_DN[0]	H42			>>EXP_C_TXN_0 (27)	
Not functional in HSW-E 28-lane SKU										
(26) EXP_A_RXP_15				BB56	PE2D_RX_DP[15]	BA47			>>EXP_A_TXP_15 (26)	
(26) EXP_A_RXP_14				BA57	PE2D_RX_DP[14]	AY48			>>EXP_A_TXP_14 (26)	
(26) EXP_A_RXP_13				AT56	PE2D_RX_DP[13]	BA49			>>EXP_A_TXP_13 (26)	
(26) EXP_A_RXP_12				AV58	PE2D_RX_DP[12]	AY50			>>EXP_A_TXP_12 (26)	
(26) EXP_A_RXN_15				AY56	PE2D_RX_DN[15]	AW47			>>EXP_A_TXN_15 (26)	
(26) EXP_A_RXN_14				AY58	PE2D_RX_DN[14]	AV48			>>EXP_A_TXN_14 (26)	
(26) EXP_A_RXN_13				AP56	PE2D_RX_DN[13]	AW49			>>EXP_A_TXN_13 (26)	
(26) EXP_A_RXN_12				AT58	PE2D_RX_DN[12]	AV50			>>EXP_A_TXN_12 (26)	
(26) EXP_A_RXP_11				AU57	PE2C_RX_DP[11]	BA51			>>EXP_A_TXP_11 (26)	
(26) EXP_A_RXP_10				AL57	PE2C_RX_DP[10]	BB54			>>EXP_A_TXP_10 (26)	
(26) EXP_A_RXP_9				AM58	PE2C_RX_DP[9]	BA53			>>EXP_A_TXP_9 (26)	
(26) EXP_A_RXP_8				AK56	PE2C_RX_DP[8]	AY52			>>EXP_A_TXP_8 (26)	
(26) EXP_A_RXN_11				AR57	PE2C_RX_DN[11]	AW51			>>EXP_A_TXN_11 (26)	
(26) EXP_A_RXN_10				AJ57	PE2C_RX_DN[10]	AY54			>>EXP_A_TXN_10 (26)	
(26) EXP_A_RXN_9				AK58	PE2C_RX_DN[9]	AW53			>>EXP_A_TXN_9 (26)	
(26) EXP_A_RXN_8				AK56	PE2C_RX_DN[8]	AV52			>>EXP_A_TXN_8 (26)	
(26) EXP_A_RXP_7				AF58	PE2B_RX_DP[7]	AT54			>>EXP_A_TXP_7 (26)	
(26) EXP_A_RXP_6				AE55	PE2B_RX_DP[6]	AR53			>>EXP_A_TXP_6 (26)	
(26) EXP_A_RXP_5				AD56	PE2B_RX_DP[5]	AK54			>>EXP_A_TXP_5 (26)	
(26) EXP_A_RXP_4				AD54	PE2B_RX_DP[4]	AJ53			>>EXP_A_TXP_4 (26)	
(26) EXP_A_RXN_7				AE57	PE2B_RX_DN[7]	AP54			>>EXP_A_TXN_7 (26)	
(26) EXP_A_RXN_6				AC55	PE2B_RX_DN[6]	AN53			>>EXP_A_TXN_6 (26)	
(26) EXP_A_RXN_5				AB56	PE2B_RX_DN[5]	AH54			>>EXP_A_TXN_5 (26)	
(26) EXP_A_RXN_4				AB54	PE2B_RX_DN[4]	AG53			>>EXP_A_TXN_4 (26)	
(26) EXP_A_RXP_3				W55	PE2A_RX_DP[3]	AP52			>>EXP_A_TXP_3 (26)	
(26) EXP_A_RXP_2				V56	PE2A_RX_DP[2]	AR51			>>EXP_A_TXP_2 (26)	
(26) EXP_A_RXP_1				V54	PE2A_RX_DP[1]	AP50			>>EXP_A_TXP_1 (26)	
(26) EXP_A_RXP_0				N55	PE2A_RX_DP[0]	AR49			>>EXP_A_TXP_0 (26)	
(26) EXP_A_RXN_3				U55	PE2A_RX_DN[3]	AM52			>>EXP_A_TXN_3 (26)	
(26) EXP_A_RXN_2				T56	PE2A_RX_DN[2]	AN51			>>EXP_A_TXN_2 (26)	
(26) EXP_A_RXN_1				T54	PE2A_RX_DN[1]	AM50			>>EXP_A_TXN_1 (26)	
(26) EXP_A_RXN_0				L55	PE2A_RX_DN[0]	AN49			>>EXP_A_TXN_0 (26)	

CZIF-SOCKET2011-RH-5

CPU1G

HASWELL-E

(23) EXP_B_RXP_15				AR45	PE3D_RX_DP[15]	P44			>>EXP_B_TXP_15 (23)	
(23) EXP_B_RXP_14				AP46	PE3D_RX_DP[14]	AA43			>>EXP_B_TXP_14 (23)	
(23) EXP_B_RXP_13				AR47	PE3D_RX_DP[13]	AB44			>>EXP_B_TXP_13 (23)	
(23) EXP_B_RXP_12				AJ47	PE3D_RX_DP[12]	AC45			>>EXP_B_TXP_12 (23)	
(23) EXP_B_RXN_15				AN45	PE3D_RX_DN[15]	T44			>>EXP_B_TXN_15 (23)	
(23) EXP_B_RXN_14				AM46	PE3D_RX_DN[14]	AC43			>>EXP_B_TXN_14 (23)	
(23) EXP_B_RXN_13				AN47	PE3D_RX_DN[13]	Y44			>>EXP_B_TXN_13 (23)	
(23) EXP_B_RXN_12				AG47	PE3D_RX_DN[12]	AA45			>>EXP_B_TXN_12 (23)	
(23) EXP_B_RXP_11				AJ49	PE3C_RX_DP[11]	AB46			>>EXP_B_TXP_11 (23)	
(23) EXP_B_RXP_10				AH50	PE3C_RX_DP[10]	AC47			>>EXP_B_TXP_10 (23)	
(23) EXP_B_RXP_9				AH48	PE3C_RX_DP[9]	U45			>>EXP_B_TXP_9 (23)	
(23) EXP_B_RXP_8					PE3C_RX_DP[8]	T46			>>EXP_B_TXP_8 (23)	
(23) EXP_B_RXN_11				AG49	PE3C_RX_DN[11]	Y46			>>EXP_B_TXN_11 (23)	
(23) EXP_B_RXN_10				AF50	PE3C_RX_DN[10]	AA47			>>EXP_B_TXN_10 (23)	
(23) EXP_B_RXN_9				AG51	PE3C_RX_DN[9]	R45			>>EXP_B_TXN_9 (23)	
(23) EXP_B_RXN_8				AF48	PE3C_RX_DN[8]	P46			>>EXP_B_TXN_8 (23)	
(24) EXP_B_RXP_7				AC51	PE3B_RX_DP[7]	U49			>>EXP_B_TXP_7 (24)	
(24) EXP_B_RXP_6				AC53	PE3B_RX_DP[6]	T50			>>EXP_B_TXP_6 (24)	
(24) EXP_B_RXP_5				AB52	PE3B_RX_DP[5]	U51			>>EXP_B_TXP_5 (24)	
(24) EXP_B_RXP_4				AB50	PE3B_RX_DP[4]	T52			>>EXP_B_TXP_4 (24)	
(24) EXP_B_RXN_7				AA51	PE3B_RX_DN[7]	R49			>>EXP_B_TXN_7 (24)	
(24) EXP_B_RXN_6				AA53	PE3B_RX_DN[6]	P50			>>EXP_B_TXN_6 (24)	
(24) EXP_B_RXN_5				Y52	PE3B_RX_DN[5]	R51			>>EXP_B_TXN_5 (24)	
(24) EXP_B_RXN_4				Y50	PE3B_RX_DN[4]	P52			>>EXP_B_TXN_4 (24)	
(24) EXP_B_RXP_3				AC49	PE3A_RX_DP[3]	T48			>>EXP_B_TXP_3 (24)	
(24) EXP_B_RXP_2				AH46	PE3A_RX_DP[2]	U47			>>EXP_B_TXP_2 (24)	
(24) EXP_B_RXP_1				AJ45	PE3A_RX_DP[1]	L51			>>EXP_B_TXP_1 (24)	
(24) EXP_B_RXP_0				AH44	PE3A_RX_DP[0]	K50			>>EXP_B_TXP_0 (24)	
(24) EXP_B_RXN_3				AA49	PE3A_RX_DN[3]	P48			>>EXP_B_TXN_3 (24)	
(24) EXP_B_RXN_2				AE46	PE3A_RX_DN[2]	R47			>>EXP_B_TXN_2 (24)	
(24) EXP_B_RXN_1				AG45	PE3A_RX_DN[1]	J51			>>EXP_B_TXN_1 (24)	
(24) EXP_B_RXN_0				AF44	PE3A_RX_DN[0]	H50			>>EXP_B_TXN_0 (24)	

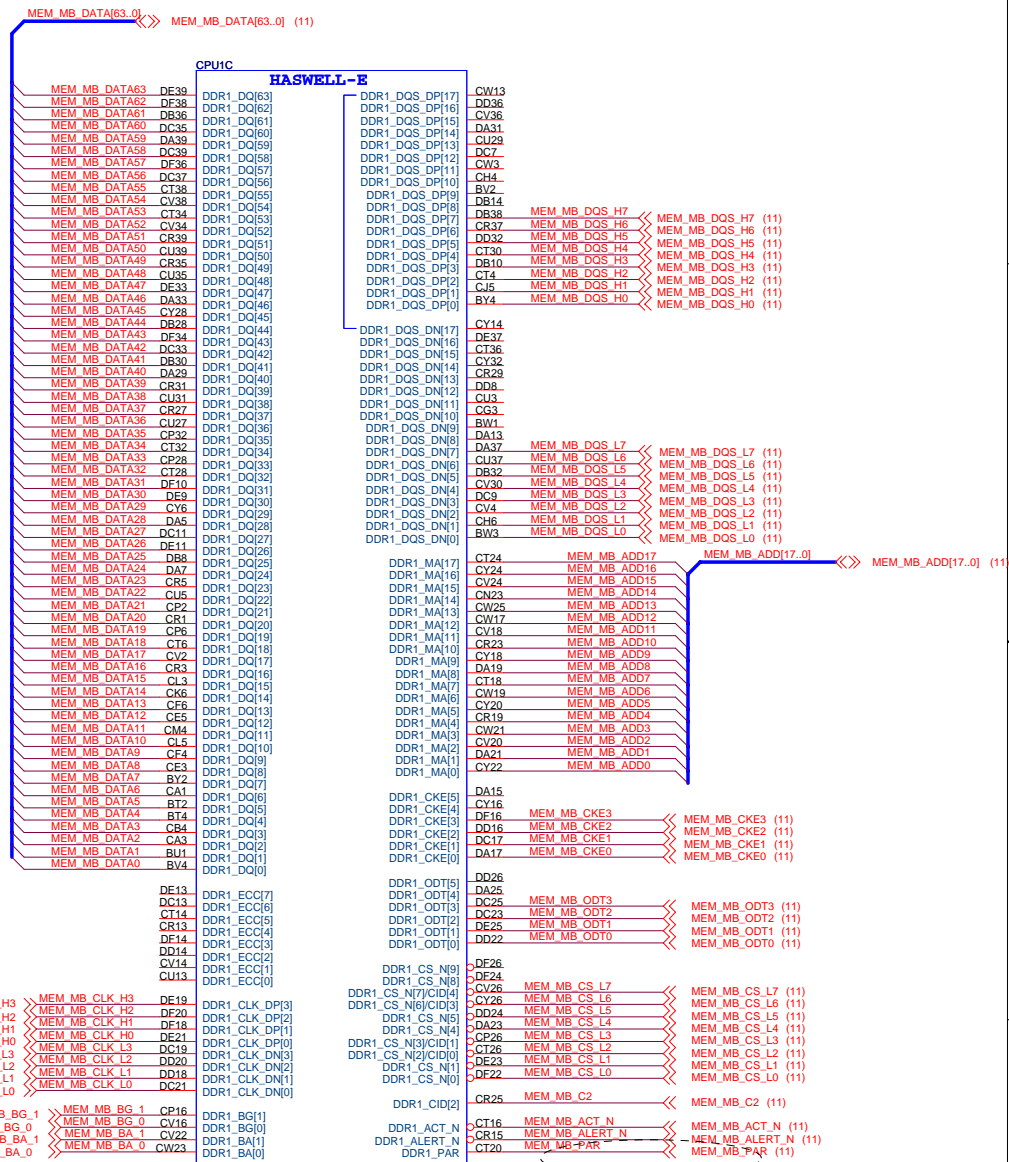
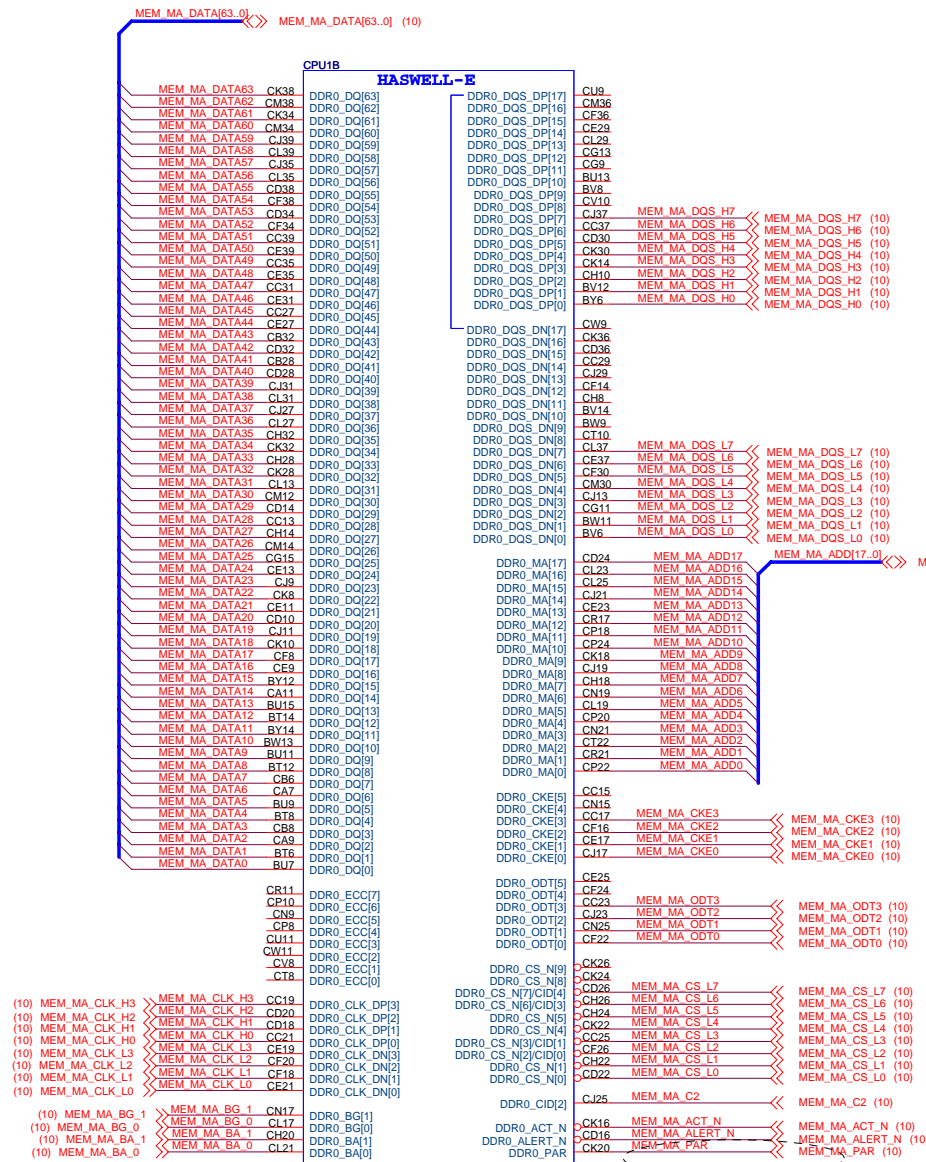
CZIF-SOCKET2011-RH-5



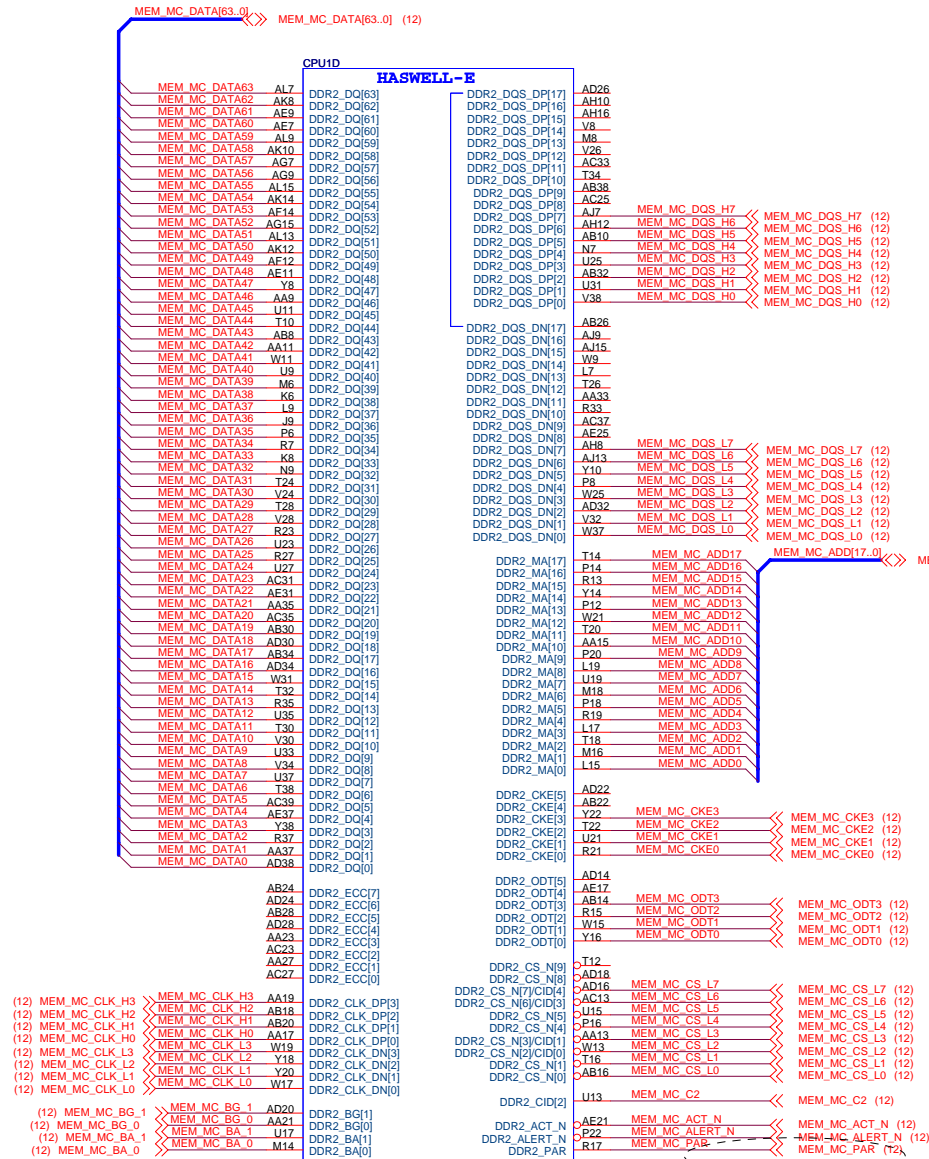
MICRO-STAR INT'L CO.,LTD

MS-7882

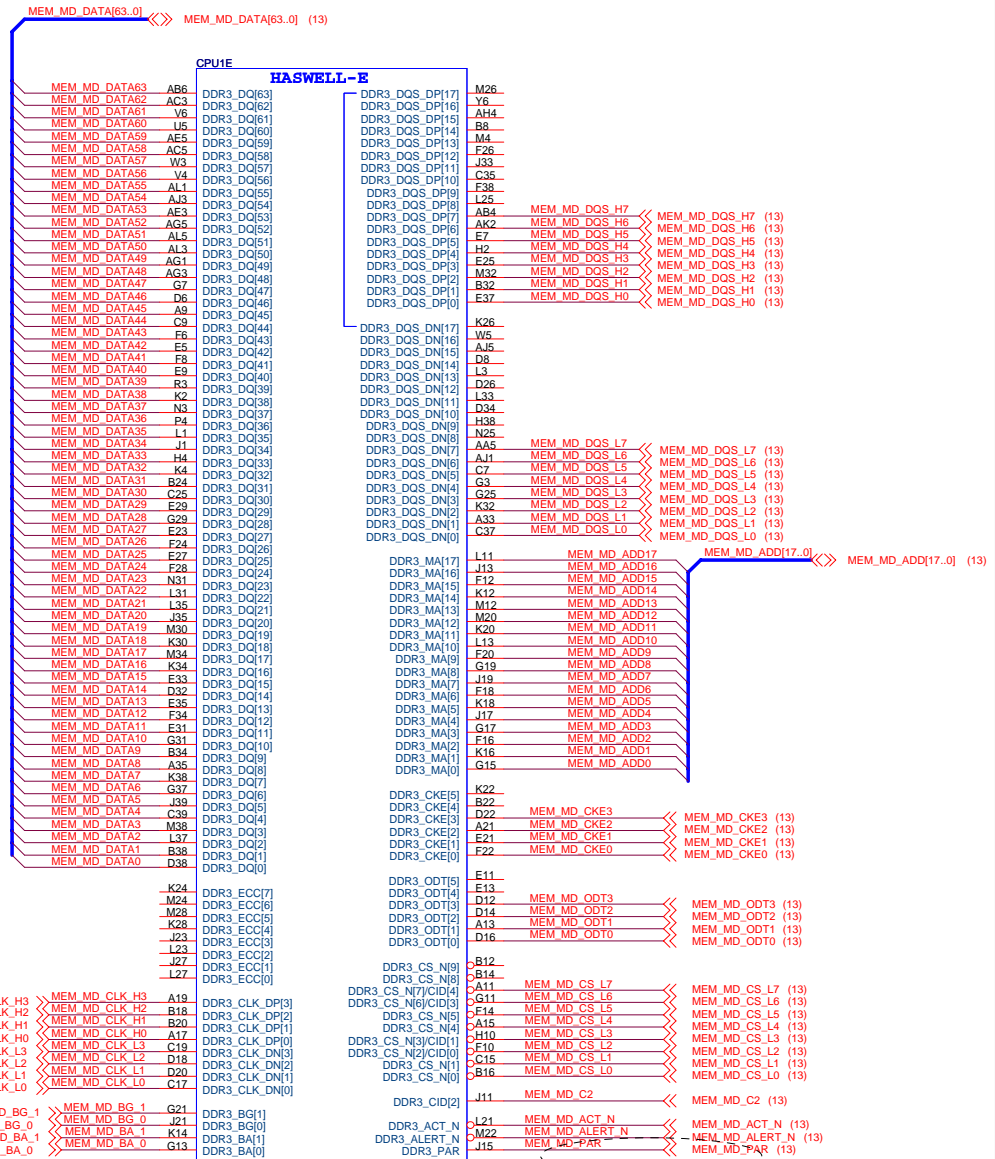
Size Custom	Document Description CPU-DMI/PEG	Rev 1.0
Date: Thursday, June 26, 2014	Sheet 4	of 66



CPU-Memory2/3



CZIF-SOCKET2011-RH-5



CZIF-SOCKET2011-RH-5



MICRO-STAR INT'L CO.,LTD

MS-7882

Size	Document Description	Rev
Custom	CPU-Memory2/3	1.0
Date: Thursday, June 26, 2014		Sheet 6 of 66

CPU-GND

CPU1N

HASWELL-E

A23	VSS-629	M2	VSS-553	M36	VSS-472
A37	VSS-628	M2	VSS-551	M42	VSS-480
A39	VSS-627	M2	VSS-550	M42	VSS-471
A41	VSS-626	M2	VSS-549	M44	VSS-470
A43	VSS-625	M2	VSS-548	M46	VSS-469
A45	VSS-624	M2	VSS-547	M48	VSS-467
A47	VSS-623	M2	VSS-546	M50	VSS-466
A49	VSS-622	M2	VSS-545	M52	VSS-468
A5	VSS-621	M2	VSS-544	M52	VSS-465
A51	VSS-620	M2	VSS-543	M52	VSS-464
A7	VSS-619	M2	VSS-541	N29	VSS-463
B10	VSS-618	M2	VSS-540	N33	VSS-462
B36	VSS-617	M2	VSS-539	N35	VSS-461
B40	VSS-616	M2	VSS-538	N37	VSS-460
B52	VSS-615	M2	VSS-537	N39	VSS-459
B6	VSS-614	M2	VSS-536	N43	VSS-458
C33	VSS-613	M2	VSS-535	N45	VSS-457
C5	VSS-612	M2	VSS-534	N47	VSS-456
C55	VSS-611	M2	VSS-533	N49	VSS-455
D10	VSS-610	M2	VSS-532	N5	VSS-454
D24	VSS-609	M2	VSS-531	N51	VSS-452
D36	VSS-612	M2	VSS-530	N53	VSS-451
D4	VSS-608	M2	VSS-529	P24	VSS-450
D40	VSS-607	M2	VSS-528	P26	VSS-449
E1	VSS-606	M2	VSS-527	P28	VSS-448
E39	VSS-605	M2	VSS-526	P30	VSS-447
E41	VSS-604	M2	VSS-525	P32	VSS-446
F2	VSS-603	M2	VSS-524	P34	VSS-445
F30	VSS-602	M2	VSS-523	P36	VSS-444
F32	VSS-601	M2	VSS-522	P40	VSS-443
F36	VSS-600	M2	VSS-521	P54	VSS-442
F4	VSS-599	M2	VSS-520	P56	VSS-441
F42	VSS-598	M2	VSS-517	R11	VSS-440
F44	VSS-597	M2	VSS-516	R25	VSS-439
F48	VSS-596	M2	VSS-515	R29	VSS-438
F50	VSS-595	M2	VSS-514	R31	VSS-437
G1	VSS-594	M2	VSS-513	R39	VSS-436
G23	VSS-593	M2	VSS-512	R5	VSS-435
G27	VSS-592	M2	VSS-511	R9	VSS-434
G33	VSS-591	M2	VSS-510	R9	VSS-433
G35	VSS-590	M2	VSS-509	R9	VSS-432
G39	VSS-589	M2	VSS-508	T36	VSS-431
G41	VSS-588	M2	VSS-507	T4	VSS-430
G45	VSS-587	M2	VSS-506	T6	VSS-429
G47	VSS-586	M2	VSS-505	T8	VSS-428
G49	VSS-585	M2	VSS-504	U29	VSS-427
G5	VSS-584	M2	VSS-503	U3	VSS-426
G51	VSS-583	M2	VSS-502	U39	VSS-425
G53	VSS-582	M2	VSS-501	U41	VSS-424
G57	VSS-581	M2	VSS-500	U43	VSS-423
G9	VSS-580	M2	VSS-499	U7	VSS-422
H24	VSS-579	M2	VSS-498	U10	VSS-421
H26	VSS-578	M2	VSS-497	V12	VSS-420
H32	VSS-577	M2	VSS-496	V36	VSS-419
H34	VSS-576	M2	VSS-495	V44	VSS-418
H36	VSS-575	M2	VSS-494	V46	VSS-417
H40	VSS-574	M2	VSS-493	V50	VSS-416
H54	VSS-573	M2	VSS-492	V52	VSS-415
H6	VSS-572	M2	VSS-491	W23	VSS-414
H8	VSS-571	M2	VSS-490	W27	VSS-413
J25	VSS-570	M2	VSS-489	W33	VSS-412
J29	VSS-569	M2	VSS-488	W35	VSS-411
J3	VSS-568	M2	VSS-487	W39	VSS-410
J31	VSS-567	M2	VSS-486	W43	VSS-409
J37	VSS-566	M2	VSS-485	W45	VSS-408
J5	VSS-565	M2	VSS-484	W47	VSS-407
J53	VSS-564	M2	VSS-483	W49	VSS-406
J7	VSS-563	M2	VSS-482	W51	VSS-405
K10	VSS-562	M2	VSS-481	W53	VSS-404
K36	VSS-561	M2	VSS-480	Y12	VSS-403
K40	VSS-560	M2	VSS-479	Y17	VSS-402
L29	VSS-559	M2	VSS-478	Y26	VSS-401
L39	VSS-558	M2	VSS-477	Y28	VSS-400
L41	VSS-557	M2	VSS-476	Y30	VSS-399
L5	VSS-556	M2	VSS-475	Y32	VSS-398
M10	VSS-555	M2	VSS-474	Y34	VSS-397
	VSS-552	M2	VSS-473	Y36	VSS-396
		M2	VSS-472	Y42	VSS-395

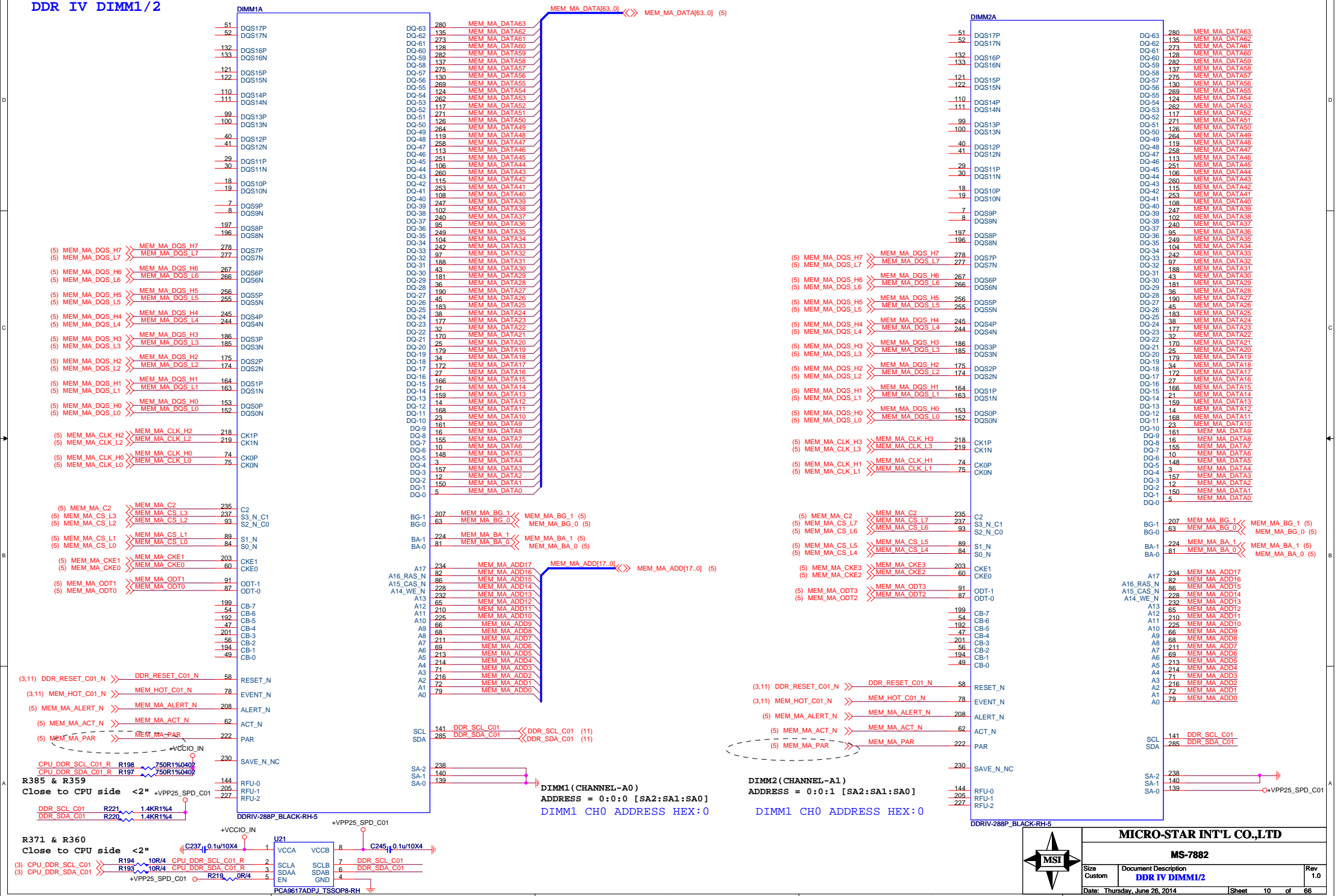
CZIF-SOCKET2011-RH-5

CPU1O

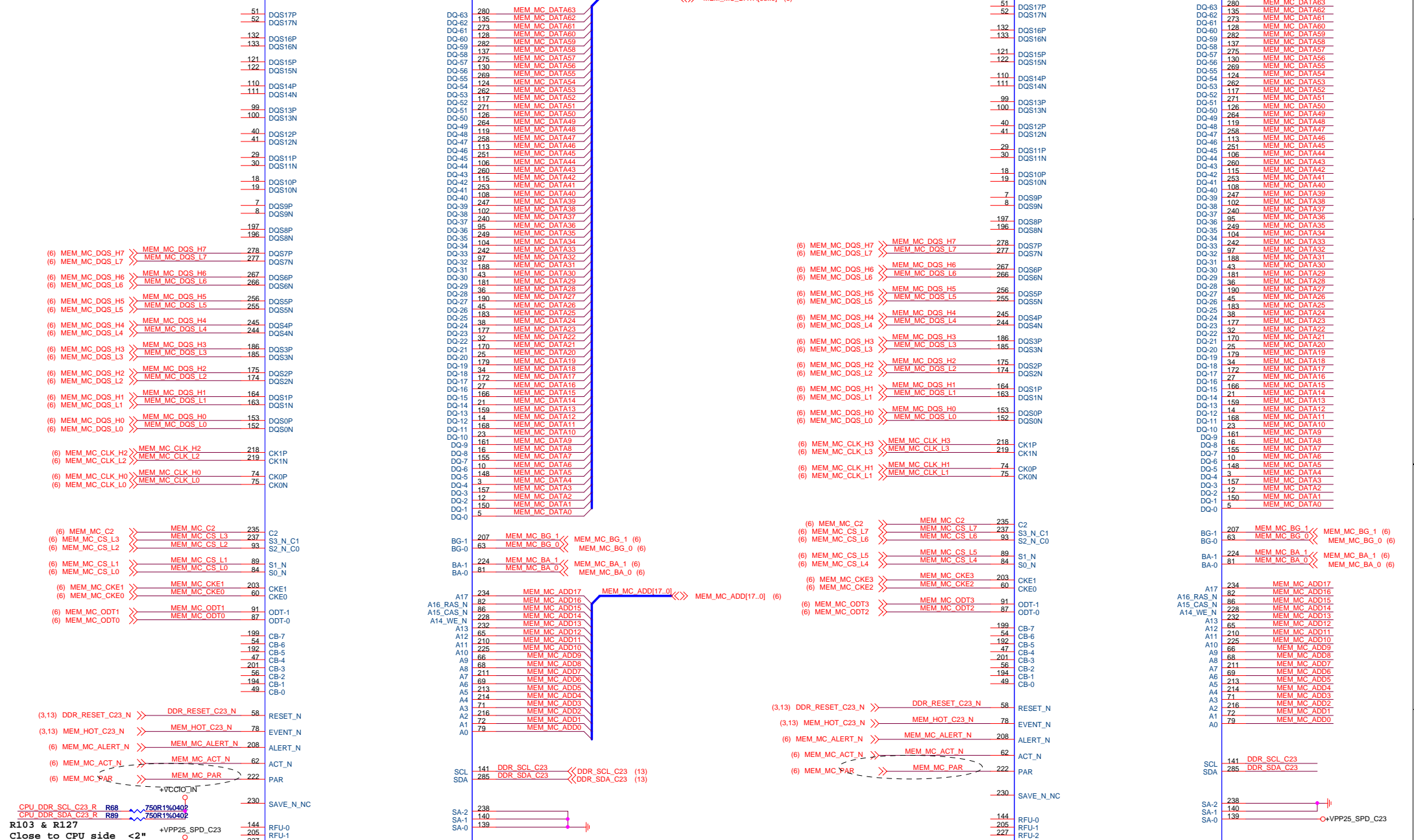
HASWELL-E

Y36	VSS-472	AH6	VSS-394	AH14
Y4	VSS-480	AH6	VSS-393	AH14
Y42	VSS-471	AH6	VSS-392	AH14
Y56	VSS-470	AH6	VSS-391	AH14
AA3	VSS-469	AH6	VSS-390	AH17
AA25	VSS-467	AH6	VSS-389	AH4
AA29	VSS-466	AH6	VSS-388	AH6
AA7	VSS-468	AH6	VSS-387	AH18
AA31	VSS-465	AH6	VSS-386	AH2
AA39	VSS-464	AH6	VSS-385	AH44
AA55	VSS-463	AH6	VSS-384	AH46
AB12	VSS-462	AH6	VSS-383	AH48
AB36	VSS-461	AH6	VSS-382	AH50
AB40	VSS-460	AH6	VSS-381	AH52
AB42	VSS-459	AH6	VSS-380	AH11
AC7	VSS-458	AH6	VSS-379	AH43
AC9	VSS-457	AH6	VSS-378	AH45
AC11	VSS-456	AH6	VSS-377	AH47
AC29	VSS-455	AH6	VSS-376	AH49
AD4	VSS-454	AH6	VSS-375	AH51
AD8	VSS-452	AH6	VSS-374	AH53
AD10	VSS-451	AH6	VSS-373	AM2
AD12	VSS-450	AH6	VSS-372	AM4
AD36	VSS-449	AH6	VSS-371	AM6
AD40	VSS-448	AH6	VSS-370	AM8
AD42	VSS-447	AH6	VSS-369	AM10
AD44	VSS-446	AH6	VSS-368	AM12
AD46	VSS-445	AH6	VSS-367	AM14
AD48	VSS-444	AH6	VSS-366	AM16
AD50	VSS-443	AH6	VSS-365	AM56
AD52	VSS-442	AH6	VSS-364	AN1
AE13	VSS-441	AH6	VSS-363	AN3
AE15	VSS-440	AH6	VSS-362	AN5
AE19	VSS-439	AH6	VSS-361	AN9
AE23	VSS-438	AH6	VSS-360	AN13
AE27	VSS-437	AH6	VSS-359	AN15
AE29	VSS-436	AH6	VSS-358	AN5
AE33	VSS-435	AH6	VSS-357	AN57
AE35	VSS-434	AH6	VSS-356	AP2
AE36	VSS-433	AH6	VSS-355	AP4
AE39	VSS-432	AH6	VSS-354	AP58
AE41	VSS-431	AH6	VSS-353	AH74
AE43	VSS-430	AH6	VSS-352	AH76
AE47	VSS-429	AH6	VSS-351	AH78
AE49	VSS-428	AH6	VSS-350	AH80
AF10	VSS-427	AH6	VSS-349	AH82
AF16	VSS-426	AH6	VSS-348	AH84
AF18	VSS-425	AH6	VSS-347	AH86
AF21	VSS-424	AH6	VSS-346	AH88
AF23	VSS-423	AH6	VSS-345	AH90
AF25	VSS-422	AH6	VSS-344	AH92
AF27	VSS-421	AH6	VSS-343	AH94
AF29	VSS-420	AH6	VSS-342	AH96
AF30	VSS-419	AH6	VSS-341	AH98
AF32	VSS-418	AH6	VSS-340	AH100
AF34	VSS-417	AH6	VSS-339	AH102
AF36	VSS-416	AH6	VSS-338	AH104
AF38	VSS-415	AH6	VSS-337	AH106
AF40	VSS-414	AH6	VSS-336	AH108
AF42	VSS-413	AH6	VSS-335	AH110
AF44	VSS-412	AH6	VSS-334	AH112
AF46	VSS-411	AH6	VSS-333	AH114
AF48	VSS-410	AH6	VSS-332	AH116
AF50	VSS-409	AH6	VSS-331	AH118
AF52	VSS-408	AH6	VSS-330	AH120
AF54	VSS-407	AH6	VSS-329	AH122
AF56	VSS-406	AH6	VSS-328	AH124
AG11	VSS-405	AH6	VSS-327	AH126
AG13	VSS-404	AH6	VSS-326	AH128
AG17	VSS-403	AH6	VSS-325	AH130
AG19	VSS-402	AH6	VSS-324	AH132
AG21	VSS-401	AH6	VSS-323	AH134
AG25	VSS-400	AH6	VSS-322	AH136
AG31	VSS-399	AH6	VSS-321	AH138
AG33	VSS-398	AH6	VSS-320	AH140
AG35	VSS-397	AH6	VSS-319	BH82
AG37	VSS-396	AH6	VSS-318	BH84
AG57	VSS-395	AH6	VSS-317	BH86
AH2	VSS-394	AH6	VSS-316	BH88
				BH90
				BH92
				BH94
				BH96
				BH98
				BH100
				BH102
				BH104
				BH106
				BH108
				BH110
				BH112
				BH114
				BH116
				BH118
				BH120
				BH122
				BH124
				BH126
				BH128
				BH130
				BH132
				BH134
				BH136
				BH138
				BH140
				BH142
				BH144
				BH146
				BH148
				BH150
				BH152
				BH154
				BH156
				BH158
				BH160
				BH162
				BH164
				BH166
				BH168
				BH170
				BH172
				BH174
				BH176
				BH178
				BH180
				BH182
				BH184
				BH186
				BH188
				BH190
				BH192
				BH194
				BH196
				BH198
				BH200

DDR IV DIMM1/2



DDR IV DIMM5/6



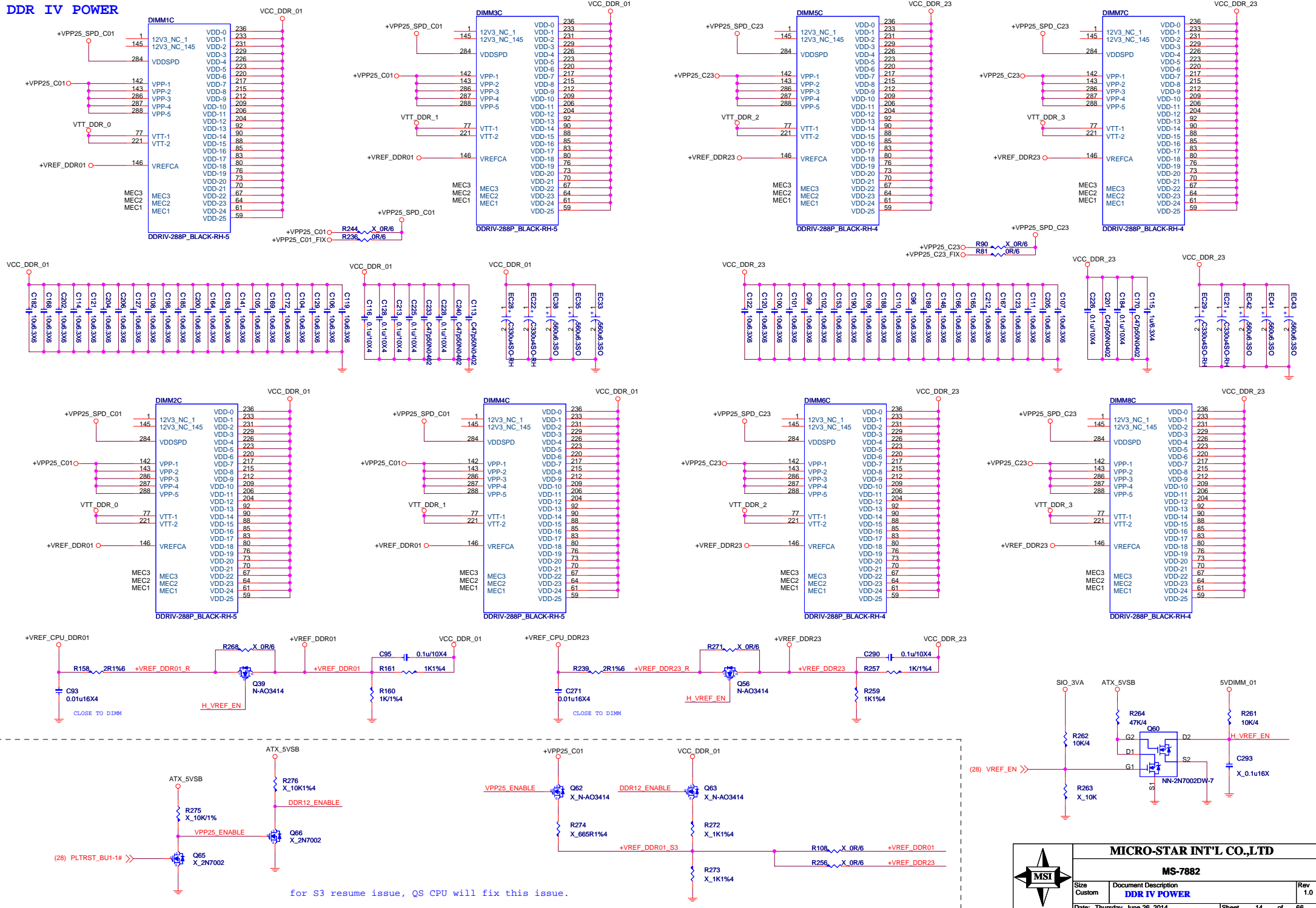
R103 & R127
Close to CPU side <2" >
CPU_DDR_SCL_C23 R88 750R1%0402
CPU_DDR_SDA_C23 R89 750R1%0402
DDR_SCL_C23 R73 1.4KR1%4
DDR_SDA_C23 R87 1.4KR1%4
+VPP25_SPD_C23
R110 & R128
Close to CPU side <2" >
(3) CPU_DDR_SCL_C23 R67 10R/4
(3) CPU_DDR_SDA_C23 R88 10R/4
+VPP25_SPD_C23 R99 0R/4

DIMM5 (CHANNEL-C0)
ADDRESS = 0:0:0 [SA2:SA1:SA0]
DIMM5 CH2 ADDRESS HEX:0

DIMM6 (CHANNEL-C1)
ADDRESS = 0:0:1 [SA2:SA1:SA0]
DIMM6 CH2 ADDRESS HEX:0

MSI
MICRO-STAR INT'L CO.,LTD
MS-7882
Size Custom Document Description
DDR IV DIMM5/6
Date: Thursday, June 26, 2014 Sheet 12 of 66

DDR IV POWER



DDR IV GND

DIMM1B			
2	VSS-93	VSS-46	147
3	VSS-92	VSS-45	149
6	VSS-91	VSS-44	151
9	VSS-90	VSS-43	154
11	VSS-89	VSS-42	156
13	VSS-88	VSS-41	158
15	VSS-87	VSS-40	160
17	VSS-86	VSS-39	162
20	VSS-85	VSS-38	165
22	VSS-84	VSS-37	167
24	VSS-83	VSS-36	169
26	VSS-82	VSS-35	173
28	VSS-81	VSS-34	174
31	VSS-80	VSS-33	176
33	VSS-79	VSS-32	178
35	VSS-78	VSS-31	180
37	VSS-77	VSS-30	182
39	VSS-76	VSS-29	184
42	VSS-75	VSS-28	187
44	VSS-74	VSS-27	189
46	VSS-73	VSS-26	191
48	VSS-72	VSS-25	193
50	VSS-71	VSS-24	195
53	VSS-70	VSS-23	198
57	VSS-69	VSS-22	200
59	VSS-68	VSS-21	202
61	VSS-67	VSS-20	209
96	VSS-66	VSS-19	241
100	VSS-65	VSS-18	243
103	VSS-64	VSS-17	245
105	VSS-63	VSS-16	248
106	VSS-62	VSS-15	250
107	VSS-61	VSS-14	252
110	VSS-60	VSS-13	254
112	VSS-59	VSS-12	257
114	VSS-58	VSS-11	259
116	VSS-57	VSS-10	261
118	VSS-56	VSS-9	263
121	VSS-55	VSS-8	265
123	VSS-54	VSS-7	268
125	VSS-53	VSS-6	270
127	VSS-52	VSS-5	272
129	VSS-51	VSS-4	274
131	VSS-50	VSS-3	276
134	VSS-49	VSS-2	279
136	VSS-48	VSS-1	281
138	VSS-47	VSS-0	283

DDRIV-288P_BLACK-RH-5

DIMM3B		
2	VSS-93	VSS-46
4	VSS-92	VSS-45
6	VSS-91	VSS-44
9	VSS-90	VSS-43
11	VSS-89	VSS-42
13	VSS-88	VSS-41
15	VSS-87	VSS-40
17	VSS-86	VSS-39
20	VSS-85	VSS-38
22	VSS-84	VSS-37
24	VSS-83	VSS-36
26	VSS-82	VSS-35
31	VSS-81	VSS-34
33	VSS-80	VSS-33
33	VSS-79	VSS-32
35	VSS-78	VSS-31
39	VSS-77	VSS-30
41	VSS-76	VSS-29
42	VSS-75	VSS-28
44	VSS-74	VSS-27
46	VSS-73	VSS-26
48	VSS-72	VSS-25
53	VSS-71	VSS-24
53	VSS-70	VSS-23
55	VSS-69	VSS-22
57	VSS-68	VSS-21
59	VSS-67	VSS-20
96	VSS-66	VSS-19
98	VSS-65	VSS-18
103	VSS-64	VSS-17
105	VSS-63	VSS-16
107	VSS-62	VSS-15
107	VSS-61	VSS-14
109	VSS-60	VSS-13
112	VSS-59	VSS-12
116	VSS-58	VSS-11
116	VSS-57	VSS-10
118	VSS-56	VSS-9
120	VSS-55	VSS-8
123	VSS-54	VSS-7
125	VSS-53	VSS-6
127	VSS-52	VSS-5
130	VSS-51	VSS-4
131	VSS-50	VSS-3
134	VSS-49	VSS-2
136	VSS-48	VSS-1
138	VSS-47	VSS-0

DDRIV-288P_BLACK-RH-5

DIMMSB		
2	VSS-93	VSS-46
4	VSS-92	VSS-45
6	VSS-91	VSS-44
8	VSS-90	VSS-43
9	VSS-89	VSS-42
11	VSS-88	VSS-41
12	VSS-80	VSS-40
15	VSS-87	VSS-39
16	VSS-86	VSS-38
17	VSS-85	VSS-37
20	VSS-84	VSS-36
24	VSS-83	VSS-35
26	VSS-82	VSS-34
28	VSS-81	VSS-33
31	VSS-79	VSS-32
35	VSS-78	VSS-31
37	VSS-77	VSS-30
42	VSS-76	VSS-29
44	VSS-75	VSS-28
46	VSS-74	VSS-27
48	VSS-73	VSS-26
50	VSS-72	VSS-25
52	VSS-71	VSS-24
53	VSS-70	VSS-23
55	VSS-69	VSS-22
57	VSS-68	VSS-21
94	VSS-67	VSS-20
96	VSS-66	VSS-19
100	VSS-65	VSS-18
103	VSS-64	VSS-17
105	VSS-63	VSS-16
106	VSS-62	VSS-15
112	VSS-61	VSS-14
114	VSS-60	VSS-13
116	VSS-59	VSS-12
118	VSS-58	VSS-11
120	VSS-57	VSS-10
121	VSS-56	VSS-9
123	VSS-55	VSS-8
127	VSS-54	VSS-7
129	VSS-53	VSS-6
130	VSS-52	VSS-5
131	VSS-51	VSS-4
139	VSS-50	VSS-3
143	VSS-49	VSS-2
136	VSS-48	VSS-1
138	VSS-47	VSS-0

DDRIV-288P BLACK-RH-4

DMM73			
2	VSS-73	VSS-46	147
4	VSS-92	VSS-45	149
6	VSS-91	VSS-44	151
9	VSS-43	VSS-43	154
11	VSS-89	VSS-42	156
13	VSS-88	VSS-41	158
15	VSS-88	VSS-41	160
17	VSS-87	VSS-40	162
20	VSS-89	VSS-39	165
22	VSS-85	VSS-38	167
26	VSS-84	VSS-37	169
28	VSS-83	VSS-36	171
30	VSS-83	VSS-36	173
32	VSS-81	VSS-34	175
33	VSS-80	VSS-33	176
34	VSS-80	VSS-33	180
35	VSS-78	VSS-31	182
37	VSS-77	VSS-30	184
42	VSS-76	VSS-29	187
43	VSS-75	VSS-28	189
44	VSS-74	VSS-27	193
46	VSS-73	VSS-26	195
48	VSS-72	VSS-25	198
50	VSS-74	VSS-24	200
53	VSS-70	VSS-23	212
55	VSS-69	VSS-22	219
57	VSS-68	VSS-21	239
94	VSS-68	VSS-20	241
96	VSS-66	VSS-19	243
98	VSS-65	VSS-18	246
101	VSS-64	VSS-17	248
103	VSS-63	VSS-16	252
105	VSS-62	VSS-15	254
112	VSS-61	VSS-14	259
116	VSS-60	VSS-13	261
118	VSS-58	VSS-12	263
119	VSS-58	VSS-11	265
120	VSS-57	VSS-10	270
121	VSS-56	VSS-9	272
123	VSS-55	VSS-8	276
125	VSS-54	VSS-7	277
126	VSS-53	VSS-6	278
127	VSS-52	VSS-5	279
129	VSS-51	VSS-4	281
131	VSS-50	VSS-3	283
134	VSS-49	VSS-2	284
136	VSS-48	VSS-1	285
137	VSS-47	VSS-0	286
138	VSS-47	VSS-0	283

DDRIV-288P BLACK-RH-4

DIM2B		
2	VSS-93	VSS-46
4	VSS-92	VSS-45
6	VSS-91	VSS-44
8	VSS-90	VSS-43
9		VSS-42
11	VSS-89	VSS-41
13	VSS-88	VSS-40
15	VSS-87	VSS-39
17	VSS-86	VSS-38
20	VSS-85	VSS-37
22	VSS-84	VSS-36
26	VSS-83	VSS-35
28	VSS-82	VSS-34
30	VSS-81	VSS-33
31	VSS-79	VSS-32
35	VSS-78	VSS-31
37	VSS-77	VSS-30
42	VSS-76	VSS-29
44	VSS-75	VSS-28
46	VSS-74	VSS-27
48	VSS-73	VSS-26
50	VSS-72	VSS-25
52	VSS-71	VSS-24
53	VSS-70	VSS-23
55	VSS-69	VSS-22
57	VSS-68	VSS-21
94	VSS-67	VSS-20
96	VSS-66	VSS-19
100	VSS-65	VSS-18
103	VSS-64	VSS-17
105	VSS-63	VSS-16
109	VSS-62	VSS-15
110	VSS-61	VSS-14
112	VSS-60	VSS-13
114	VSS-59	VSS-12
116	VSS-58	VSS-11
118	VSS-57	VSS-10
120	VSS-56	VSS-9
123	VSS-54	VSS-8
125	VSS-53	VSS-6
127	VSS-52	VSS-5
129	VSS-51	VSS-4
131	VSS-50	VSS-3
133	VSS-49	VSS-2
136	VSS-48	VSS-1
138	VSS-47	VSS-0

DDRIV-288P_BLACK-RH-5

DIMM4B			
2	VSS-93	VSS-46	147
4	VSS-92	VSS-45	149
6	VSS-90	VSS-44	151
9	VSS-89	VSS-43	154
11	VSS-88	VSS-42	156
13	VSS-87	VSS-41	158
17	VSS-86	VSS-40	160
20	VSS-85	VSS-38	162
24	VSS-84	VSS-37	165
26	VSS-83	VSS-36	167
28	VSS-82	VSS-35	169
32	VSS-81	VSS-34	171
35	VSS-79	VSS-33	173
37	VSS-78	VSS-32	176
39	VSS-77	VSS-31	178
42	VSS-76	VSS-29	180
46	VSS-75	VSS-28	182
48	VSS-74	VSS-27	184
50	VSS-73	VSS-26	187
53	VSS-72	VSS-25	189
55	VSS-71	VSS-24	191
58	VSS-70	VSS-23	193
61	VSS-69	VSS-22	195
64	VSS-68	VSS-21	198
68	VSS-67	VSS-20	200
94	VSS-66	VSS-19	202
96	VSS-65	VSS-18	239
103	VSS-64	VSS-17	241
105	VSS-63	VSS-16	243
109	VSS-62	VSS-15	246
112	VSS-61	VSS-14	250
114	VSS-60	VSS-13	252
118	VSS-59	VSS-12	254
120	VSS-57	VSS-10	257
122	VSS-56	VSS-9	259
128	VSS-55	VSS-8	261
129	VSS-54	VSS-7	263
129	VSS-53	VSS-6	265
129	VSS-52	VSS-5	268
129	VSS-51	VSS-4	270
131	VSS-50	VSS-3	272
131	VSS-49	VSS-2	274
133	VSS-48	VSS-1	276
136	VSS-47	VSS-0	279
138	VSS-47	VSS-0	281
138	VSS-47	VSS-0	283

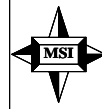
DDRIV-288P_BLACK-RH-5

DMMB6		
2	VSS-93	VSS-46
4	VSS-92	VSS-45
5	VSS-91	VSS-44
6	VSS-90	VSS-43
11	VSS-89	VSS-42
13	VSS-88	VSS-41
17	VSS-87	VSS-40
18	VSS-86	VSS-39
20	VSS-85	VSS-38
22	VSS-84	VSS-37
26	VSS-83	VSS-36
27	VSS-82	VSS-35
28	VSS-81	VSS-34
31	VSS-80	VSS-33
33	VSS-79	VSS-32
35	VSS-78	VSS-31
37	VSS-77	VSS-30
42	VSS-76	VSS-29
43	VSS-75	VSS-28
44	VSS-74	VSS-27
46	VSS-73	VSS-26
48	VSS-72	VSS-25
50	VSS-71	VSS-24
53	VSS-70	VSS-23
55	VSS-69	VSS-22
57	VSS-68	VSS-21
94	VSS-67	VSS-20
96	VSS-66	VSS-19
101	VSS-65	VSS-18
103	VSS-64	VSS-17
105	VSS-63	VSS-16
106	VSS-62	VSS-15
109	VSS-61	VSS-14
110	VSS-60	VSS-13
112	VSS-59	VSS-12
114	VSS-58	VSS-11
118	VSS-57	VSS-10
119	VSS-56	VSS-9
120	VSS-55	VSS-8
123	VSS-54	VSS-7
125	VSS-53	VSS-6
127	VSS-52	VSS-5
128	VSS-51	VSS-4
131	VSS-50	VSS-3
133	VSS-49	VSS-2
136	VSS-48	VSS-1
138	VSS-47	VSS-0

DDRIV-288P_BLACK-RH-4

DIMM8B			
2	VSS-93	VSS-46	147
3	VSS-92	VSS-45	149
4	VSS-91	VSS-44	151
5	VSS-90	VSS-43	154
6	VSS-89	VSS-42	156
11	VSS-88	VSS-41	158
13	VSS-87	VSS-40	160
15	VSS-86	VSS-39	162
20	VSS-85	VSS-38	165
22	VSS-84	VSS-37	167
24	VSS-83	VSS-36	169
26	VSS-82	VSS-35	171
28	VSS-81	VSS-34	173
31	VSS-80	VSS-33	175
33	VSS-79	VSS-32	177
35	VSS-78	VSS-31	180
37	VSS-77	VSS-30	182
42	VSS-76	VSS-29	187
44	VSS-75	VSS-28	189
44	VSS-74	VSS-27	189
46	VSS-73	VSS-26	191
48	VSS-72	VSS-25	195
50	VSS-71	VSS-24	197
53	VSS-70	VSS-23	198
55	VSS-69	VSS-22	200
94	VSS-68	VSS-21	239
96	VSS-67	VSS-20	241
96	VSS-66	VSS-19	241
98	VSS-65	VSS-18	243
101	VSS-64	VSS-17	246
103	VSS-63	VSS-16	248
105	VSS-62	VSS-15	250
107	VSS-61	VSS-14	252
112	VSS-60	VSS-13	254
114	VSS-59	VSS-12	257
116	VSS-58	VSS-11	259
118	VSS-57	VSS-10	261
120	VSS-56	VSS-9	263
122	VSS-55	VSS-8	265
123	VSS-54	VSS-7	270
126	VSS-53	VSS-6	272
127	VSS-52	VSS-5	278
129	VSS-51	VSS-4	274
131	VSS-50	VSS-3	276
134	VSS-49	VSS-2	273
136	VSS-48	VSS-1	281
138	VSS-47	VSS-0	283

DDRIV-288P_BLACK-RH-4



MICRO-STAR INT'L CO.,LTD

MS-7882

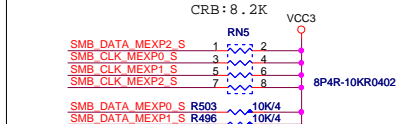
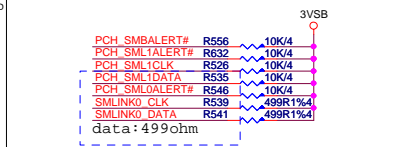
Size	Document Description
Custom	DDR IV GND

Rev	1.0
-----	-----

Date: Thursday, June 26, 2014 Sheet 15 of 66

(34) AZ_SDOUT 1 2 AZ_SDOUT R
 (34) AZ_SYNC 3 4 AZ_SYNC R
 (34) AZ_RST# 5 6 AZ_RST# R
 (34,62) AZ_BITCLK 7 8 AZ_BITCLK R

RN7 33R/6P4R



SMB DATA MEXP1 S R497 X 10K/4
LT DEBUG MODE ENABLE

```

HIGH: NORMAL MODE (DEFAULT)
LOW  : LT DEBUG MODE

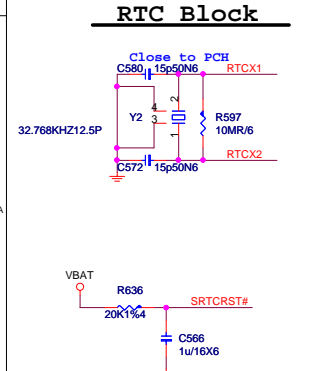
```

SMB DATA MEXP0 S R504 X 10K/4

ADR TIMER HOLD OFF (DEFENSIVE)

NOTE: EXT PU ON SMB
HIGH: NORMAL MODE (DEFAULT)

LOW : ADR TIMER HOLD OFF



32.768KHZ12.5P

C572 15p50N6

10MR/6

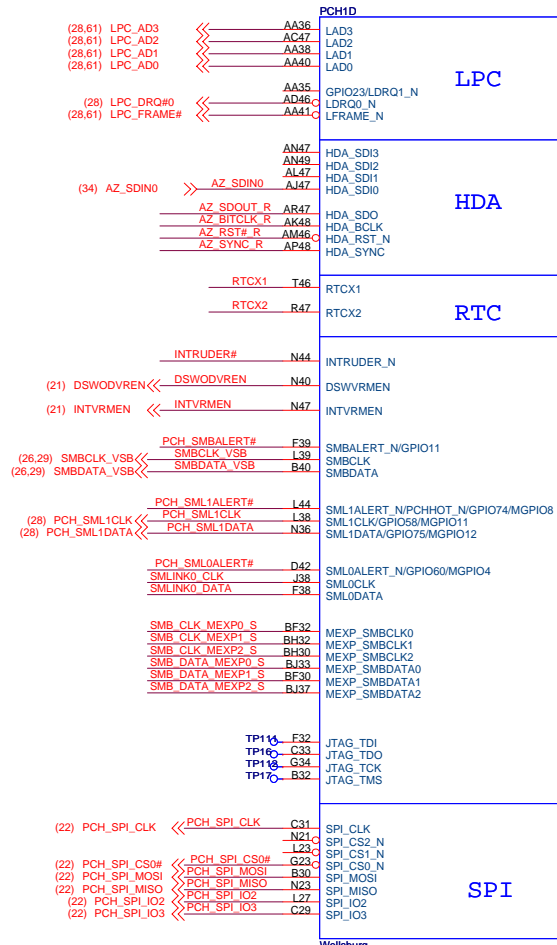
RTCX2

VBAT

R636 20K1%4

SRTCX2#

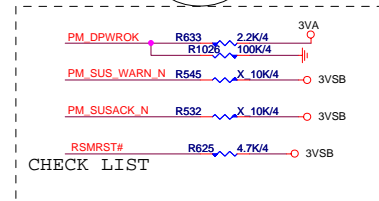
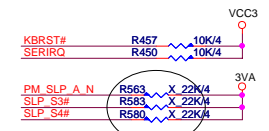
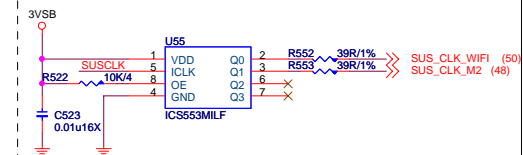
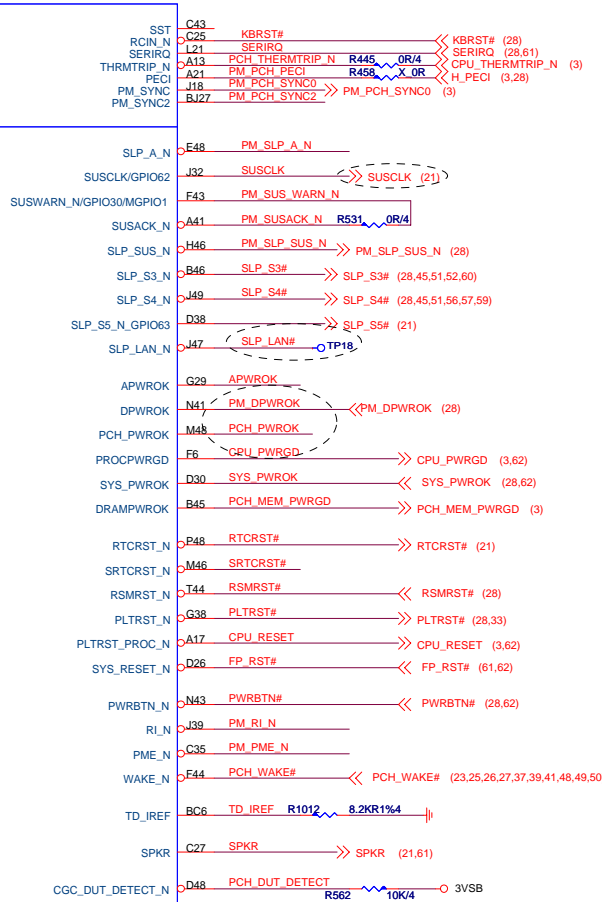
C566 1u/16X6



HDA

SPI

The negative min timing implies that DRAMPWROK must either fall before SLP_S4# or within 100 ns after it.



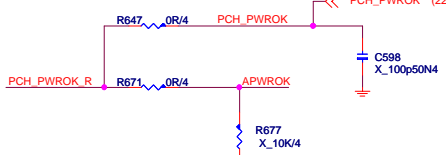
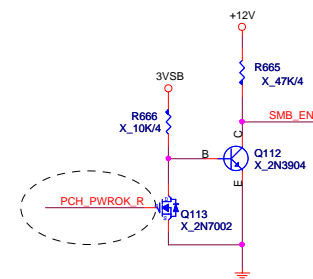
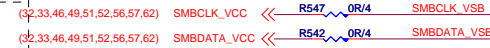
Timing diagram for the 'CHECK LIST' section. The diagram shows four signals over time:

- FP_RST#** (Red signal): Transition at R483, 2.2K/4. Terminated to 3V.
- PWRBTN#** (Blue signal): Transition at R626, X, 22K. Terminated to 3V.
- PM_RI_N** (Red signal): Transition at R534, 10K/4. Terminated to 3VSS.
- PM_PME_N** (Red signal): Transition at R510, 10K/4. Terminated to 3VSS.
- PCH_WAKE#** (Blue signal): Transition at R581, 1K/4. Terminated to 3V.

A dashed box encloses the PM_RI_N, PM_PME_N, and PCH_WAKE# signals, with a label 'CHECK LIST' below it.

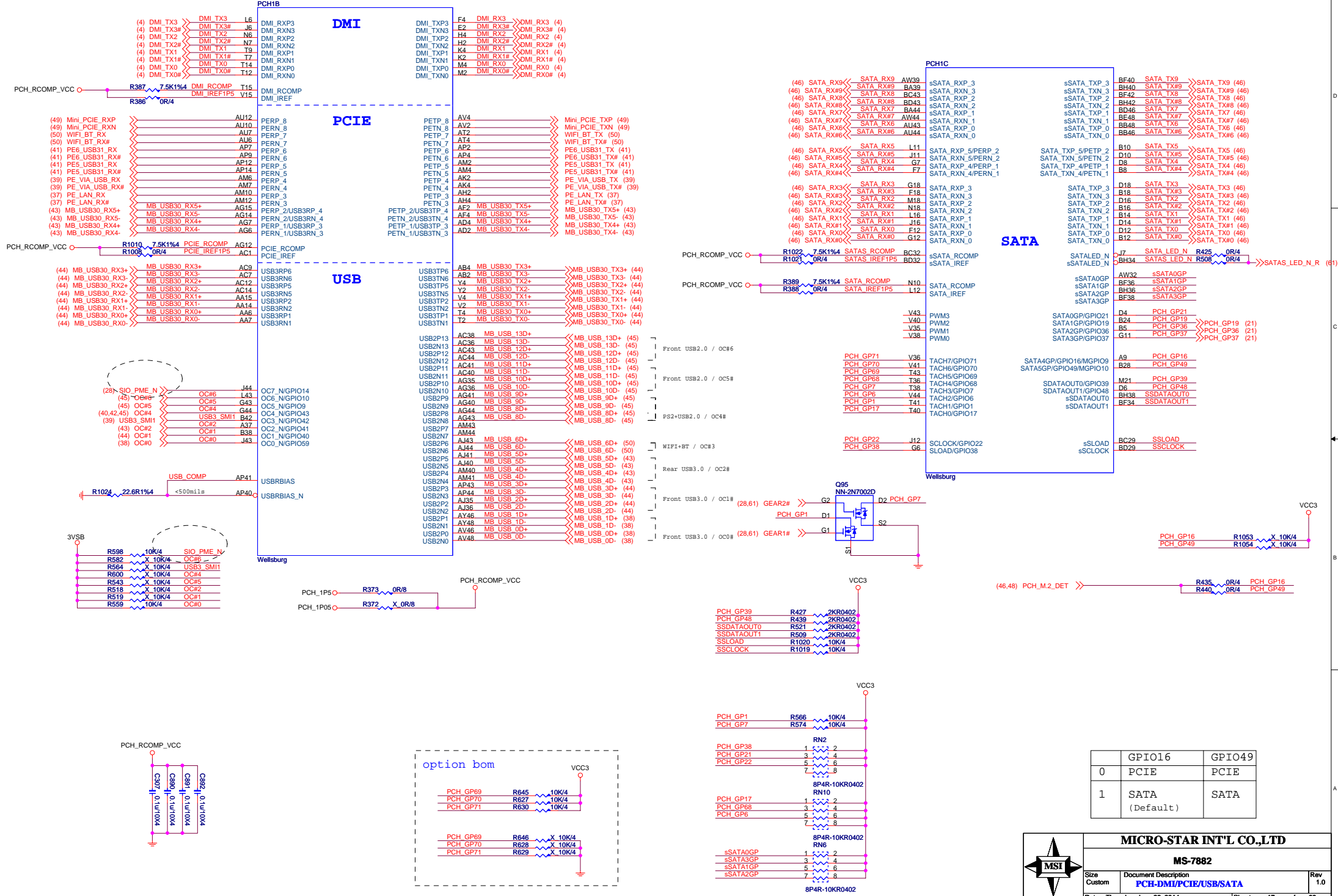


Figure 10 is a schematic diagram of the SMBus interface. It shows the connection of the X_NN-2N7002DW transistor to the SMBus lines. The base of the transistor is connected to SMBCLK_VSB. The emitter is connected to SMBCLK_VCC. The collector is connected to SMBDATA_VCC. The transistor is controlled by SMB_EN (G2) and SMB_DATA_VSB (D1). The base is also connected to SMB_DATA_VSB (G1) and SMBCLK_VSB (S2). The transistor is labeled X_NN-2N7002DW.



Trace length of APWROK must be less than PCH_PWROK

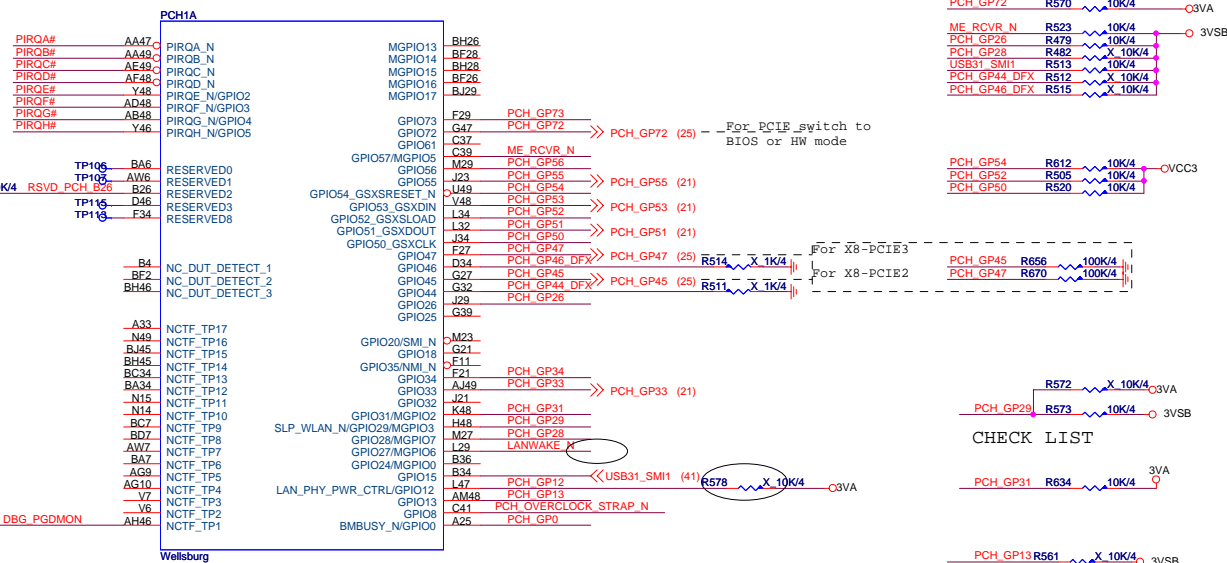
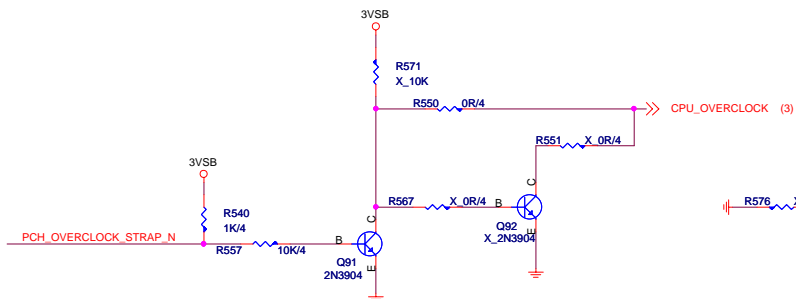
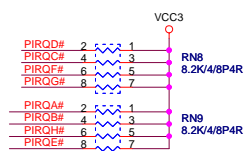
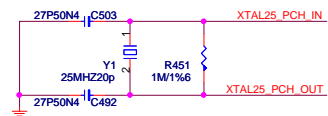
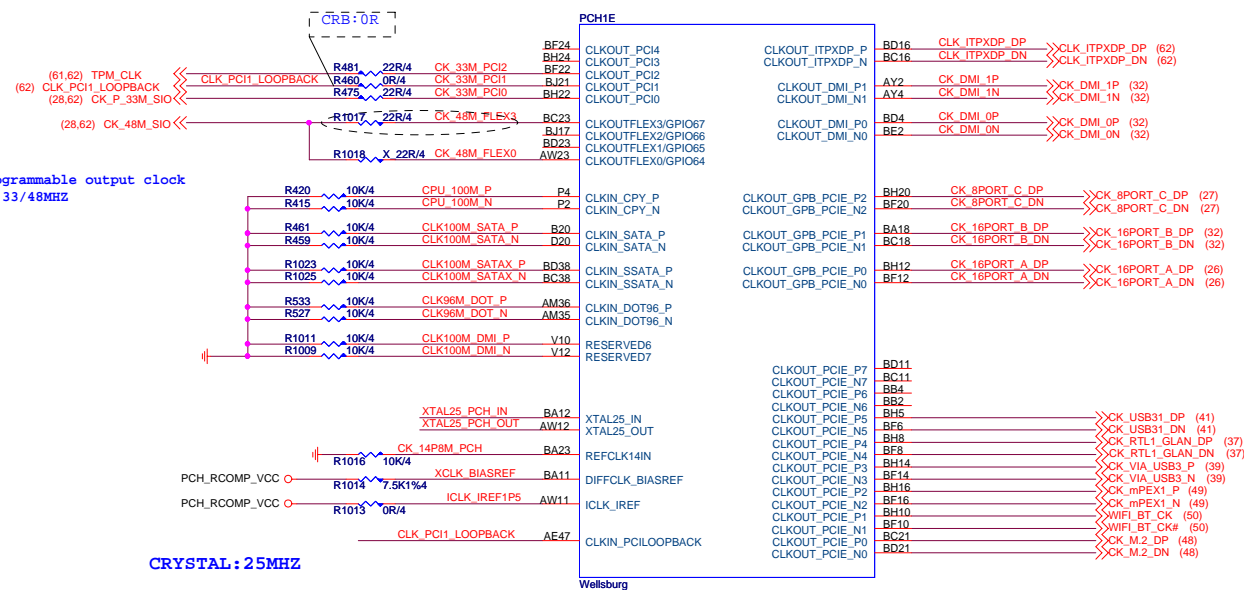
PCH-DMI/PCIE/USB/SATA



	GPIO16	GPIO49
0	PCIE	PCIE
1	SATA (Default)	SATA



PCH-CLK/GPIO



INTEGRATED CLOCK ENABLE

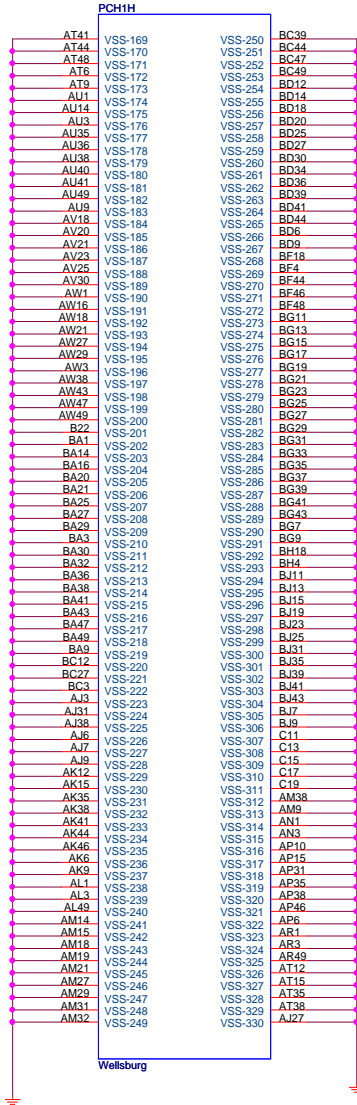
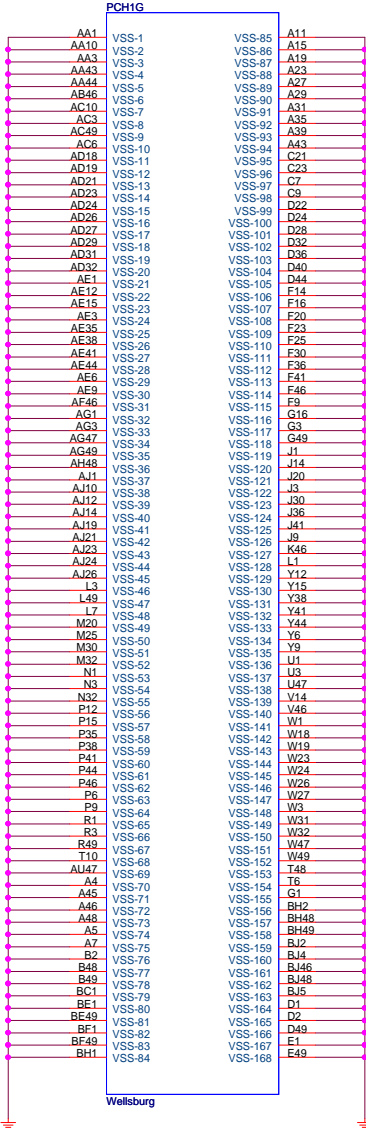
HIGH: DISABLE
LOW : ENABLE



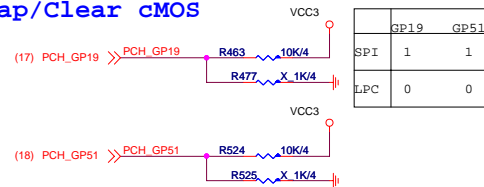
MICRO-STAR INT'L CO.,LTD

MS-7882

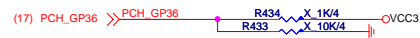
Size Custom	Document Description PCH-CLK/GPIO	Rev 1.0
Date: Thursday, June 26, 2014		Sheet 18 of 66



PCH Strap/Clear CMOS



DMI RX Termination



This signal has a weak internal pull-down.
This signal only take effect if DMI is configured in AC-coupled mode.
0 = DMI RX is terminated to VSS.
1 = option not supported.



```

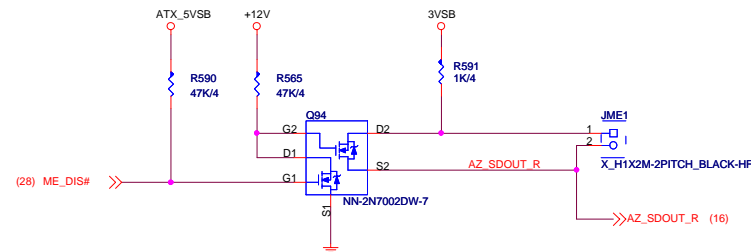
TLS CONFIDENTIALITY ENABLE STRAP
HIGH :TLS CONFIDENTIALITY ENABLE (DEFAULT)
LOW  : RING OSCILLATOR BYPASS
LOW  :TLS CONFIDENTIALITY DISABLE

```

DMI TX TERMINATION (DEFENSIVE)



This signal has a weak internal pull-down.
 This signal only takes effect if DMI is configured in DC-coupled mode.
 0 = DMI TX is terminated to VSS.
 1 = DMI TX is terminated to VCC/2.



HIGH (1-2):SECURITY MEASURES OVERRIDEN
LOW (0-1) : SECURITY PER FLASH DESCRIPTOR (DEFAULT)

DEEP SLEEP WELL ON-DIE VRM ENABLE



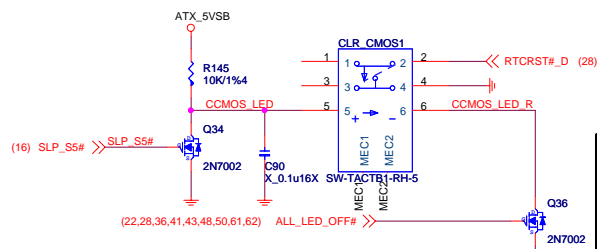
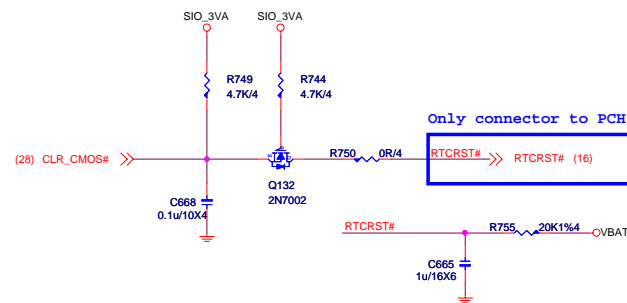
HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

LOW : REBOOT
HIGH: NO-REBOOT

NO REBOOT OPTION STRAP

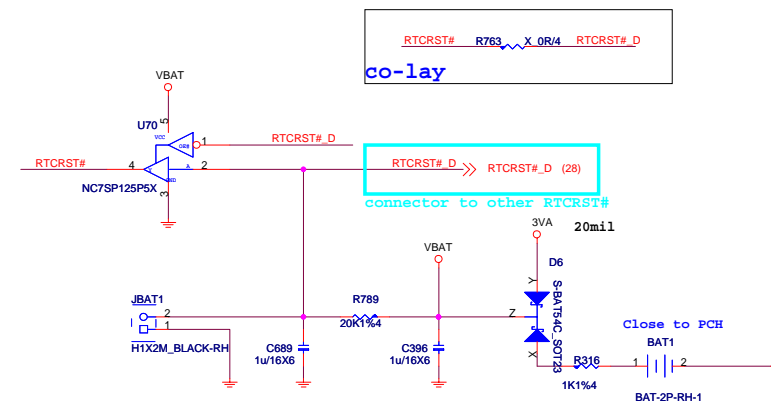


RTC and CLR_CMOS



LED LIGHTING RULE

S0/S3/S4 : LED OFF
S5 : LED ON



tri-state		
INPUT		outout pin4
PIN1	PIN2	
L	H	H
L	L	L
H	X	Z



MICRO-STAR INT'L CO.,LTD

MS-7882

Size Custom	Document Description PCH Strap/Clear cMOS	Rev 1.0
Date: Thursday, June 26, 2014		Sheet 21 of 66

(16) PCH_SPI_CS0# << PCH_SPI_CS0#

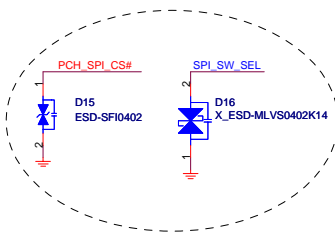
(16) PCH_SPI_MOSI << PCH_SPI_MOSI

(16) PCH_SPI_MISO << PCH_SPI_MISO

(16) PCH_SPI_CLK << PCH_SPI_CLK

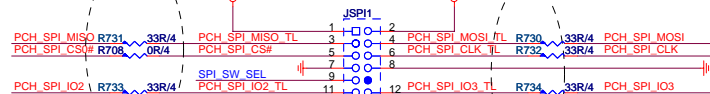
(16) PCH_SPI_IO2 << PCH_SPI_IO2

(16) PCH_SPI_IO3 << PCH_SPI_IO3



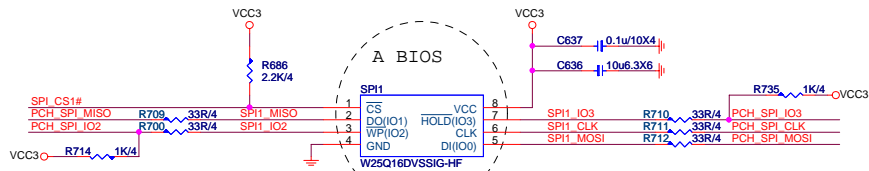
SPI DEBUG PROT

Close to SPI ROM

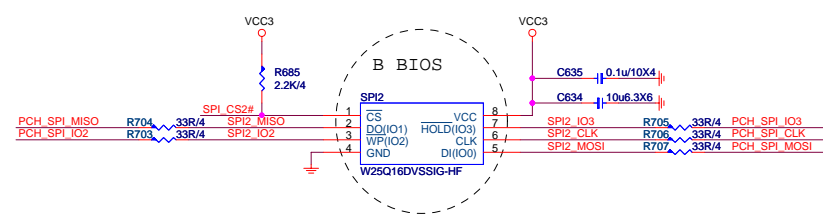


Part Number: N31-2061341-H06

(16) PCH_PWROK >> PCH_PWROK R1066 0R/4 SPI_SW_SEL 2014.06.05 Add for support TL624-1.1



16M ROM



SPI FLASH ROM

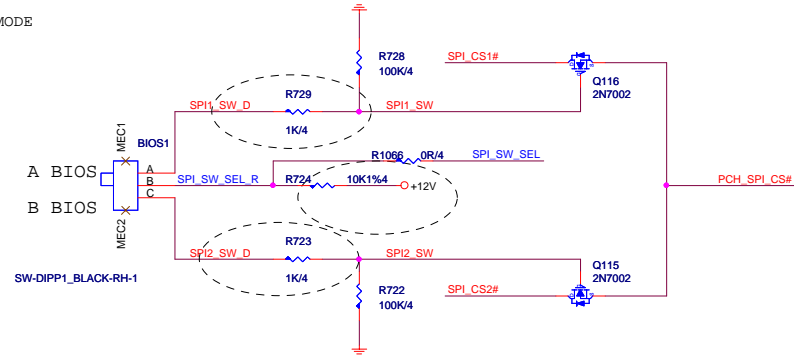
Place close to SB.

*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS# must be length matched to within 500mils.

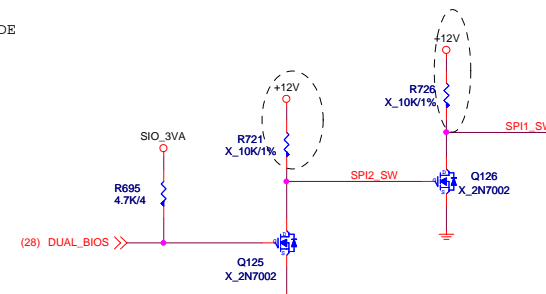
(21,28,36,41,43,48,50,61,62) ALL_LED_OFF# >>

OPTION BIOS

HW MODE



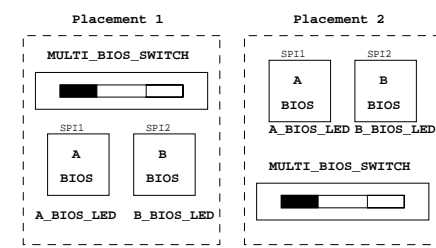
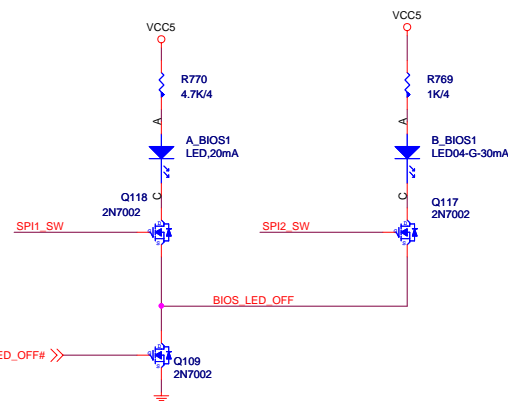
BIOS MODE



* if you not support Standby power in S5 Status, component "MULTI_BIOS_SWITCH1.B(PIN B)" Pull-high to +12V & Q12/Q13 MOS select 2N7002

* if you support Standby power in S5 Status(Ex: PCH is B75 Chipset), component "MULTI_BIOS_SWITCH1.B(PIN B)" pull-igh to ATX_5VSB, component Q12/Q13 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30



PCIE1(X16) & PCIE2(X1) slots

(25,26,27) SMBCLK_VSB_R
(25,26,27) SMBDATA_VSB_R

SMBCLK_VSB_R
SMBDATA_VSB_R

VCC3
3VSB

(16,25,26,27,37,39,41,48,49,50) PCH_WAKE#

(4) EXP_B_TXP_15
(4) EXP_B_TXN_15

(4) EXP_B_TXP_14
(4) EXP_B_TXN_14

(4) EXP_B_TXP_13
(4) EXP_B_TXN_13

(4) EXP_B_TXP_12
(4) EXP_B_TXN_12

(4) EXP_B_TXP_11
(4) EXP_B_TXN_11

(4) EXP_B_TXP_10
(4) EXP_B_TXN_10

(4) EXP_B_TXP_9
(4) EXP_B_TXN_9

(4) EXP_B_TXP_8
(4) EXP_B_TXN_8

(24) PE1_X16_TXP7
(24) PE1_X16_TXN7

(24) PE1_X16_TXP6
(24) PE1_X16_TXN6

(24) PE1_X16_TXP5
(24) PE1_X16_TXN5

(24) PE1_X16_TXP4
(24) PE1_X16_TXN4

(24) PE1_X16_TXP3
(24) PE1_X16_TXN3

(24) PE1_X16_TXP2
(24) PE1_X16_TXN2

(24) PE1_X16_TXP1
(24) PE1_X16_TXN1

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

(24) PE1_X16_TXP0
(24) PE1_X16_TXN0

PCI_E1

X2

B1

B2

B3

B4

B5

B6

B7

B8

B9

B10

B11

B12

B13

B14

B15

B16

B17

B18

B19

B20

B21

B22

B23

B24

B25

B26

B27

B28

B29

B30

B31

B32

B33

B34

B35

B36

B37

B38

B39

B40

B41

B42

B43

B44

B45

B46

B47

B48

B49

B50

B51

B52

B53

B54

B55

B56

B57

B58

B59

B60

B61

B62

B63

B64

B65

B66

B67

B68

B69

B70

B71

B72

B73

B74

B75

B76

B77

B78

B79

B80

B81

B82

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

PCI_E1

X2

B1

B2

B3

B4

B5

B6

B7

B8

B9

B10

B11

B12

B13

B14

B15

B16

B17

B18

B19

B20

B21

B22

B23

B24

B25

B26

B27

B28

B29

B30

B31

B32

B33

B34

B35

B36

B37

B38

B39

B40

B41

B42

B43

B44

B45

B46

B47

B48

B49

B50

B51

B52

B53

B54

B55

B56

B57

B58

B59

B60

B61

B62

B63

B64

B65

B66

B67

B68

B69

B70

B71

B72

B73

B74

B75

B76

B77

B78

B79

B80

B81

B82

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

X1

PCI_E1

X2

B1

B2

B3

B4

B5

B6

B7

B8

B9

B10

B11

B12

B13

B14

B15

B16

B17

B18

B19

B20

B21

B22

B23

B24

B25

B26

B27

B28

B29

B30

B31

B32

B33

B34

B35

B36

B37

B38

B39

B40

B41

B42

B43

B44

B45

B46

B47

B48

B49

B50

B51

B52

B53

B54

B55

B56

B57

B58

B59

B60

B61

B62

B63

B64

B65

B66

B67

B68

B69

B70

B71

B72

B73

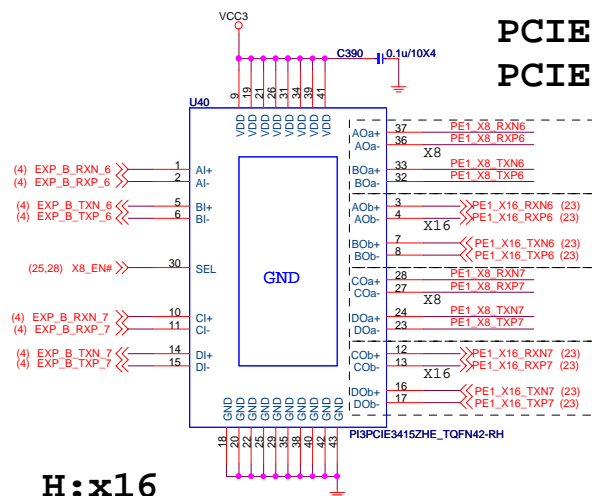
B74

B75

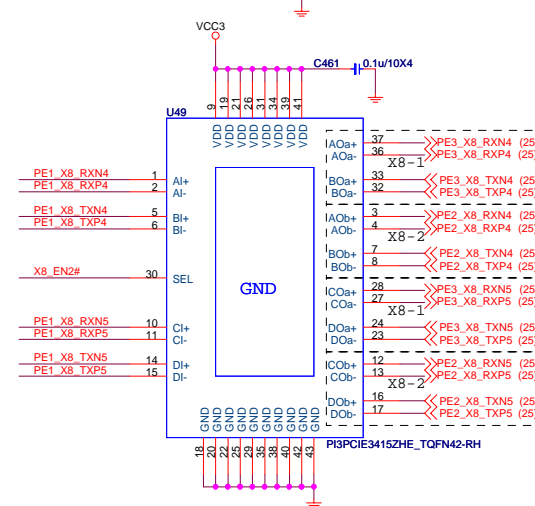
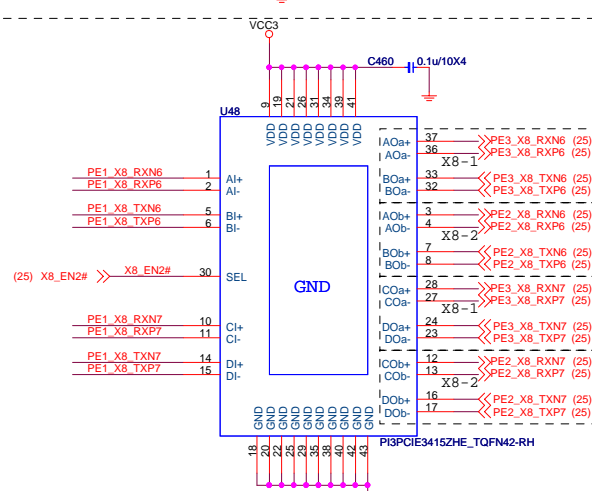
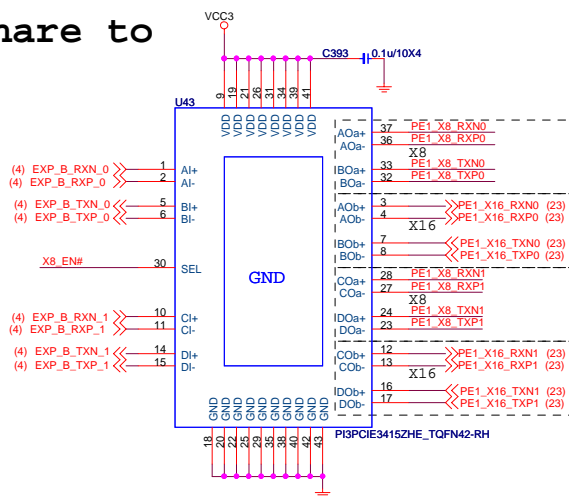
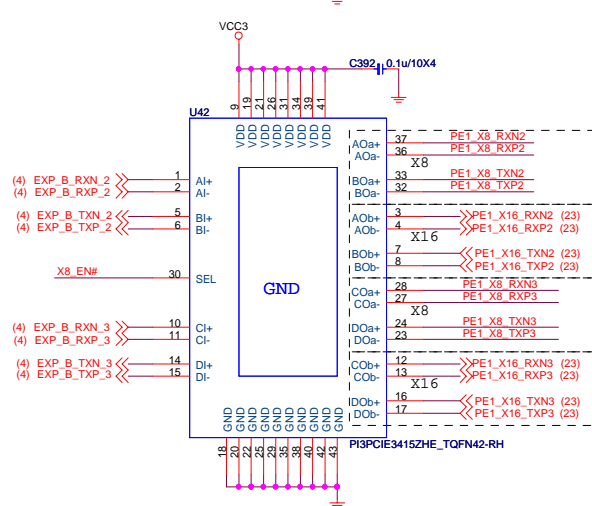
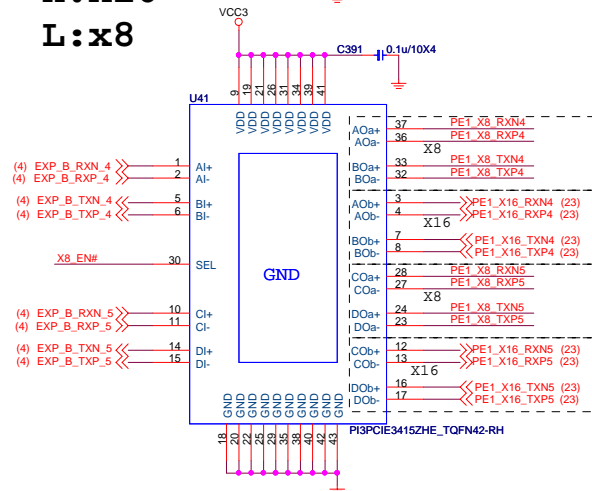
B76

B77

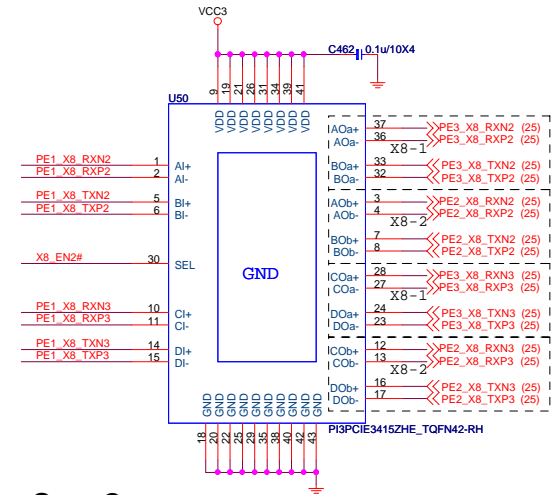
PCIE1(x16) share to
PCIE2(x8)



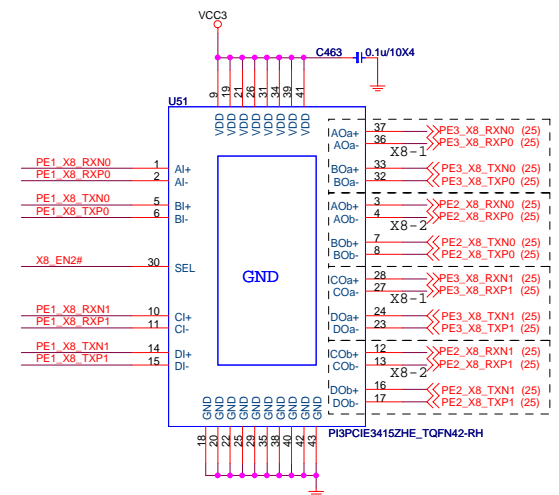
```
H:x16
L:x8
```



Switch
PCIE(x8) for PCIE2 or PCIE3



H:x8-E2
L:x8-E3

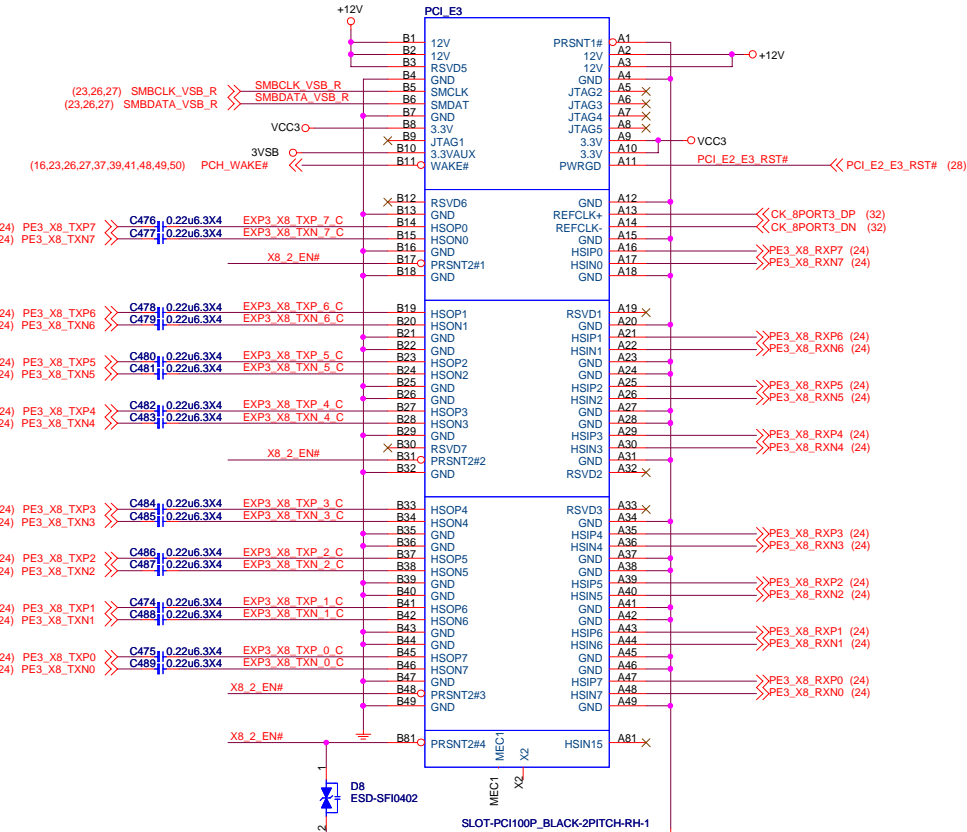
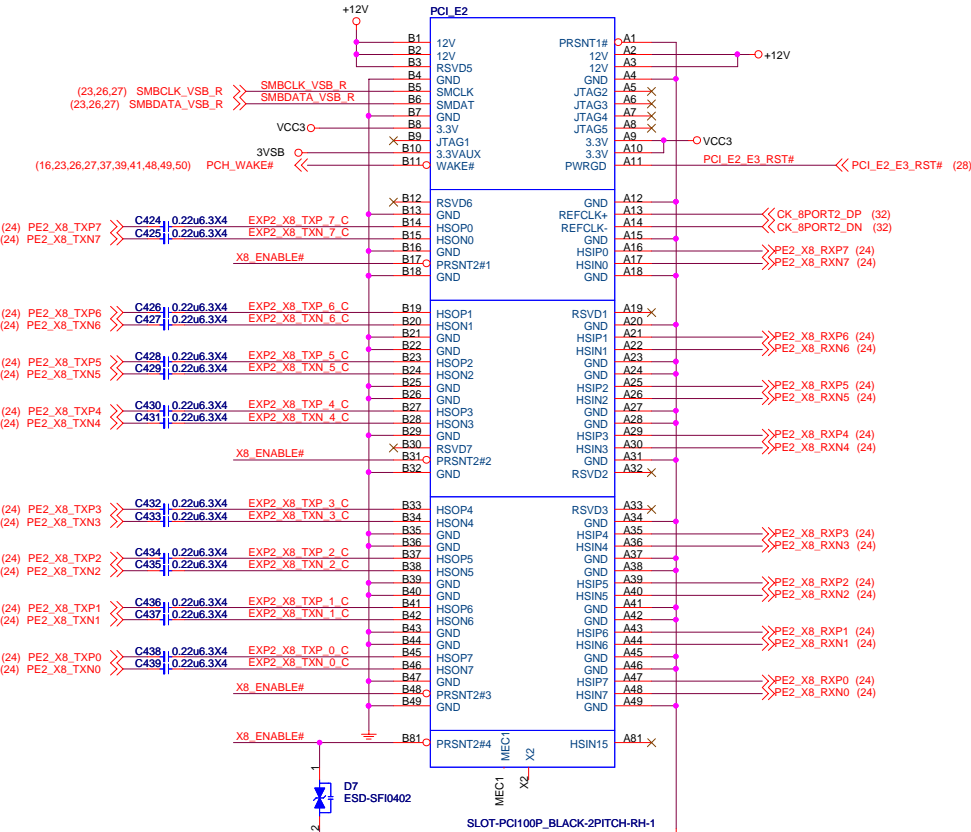


MICRO-STAR INT'L CO.,LTD

MS-7882

Size Custom	Document Description PCIE Switch 3415	Rev 1.0
Date: Thursday, June 26, 2014		Sheet 24 of 66

PCIE5(X8) /PCIE3415

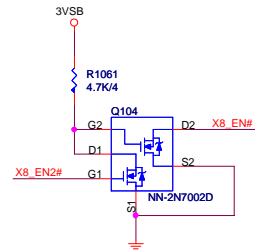
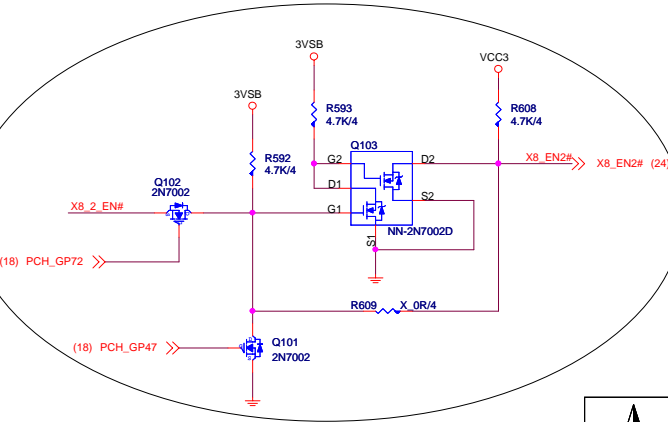
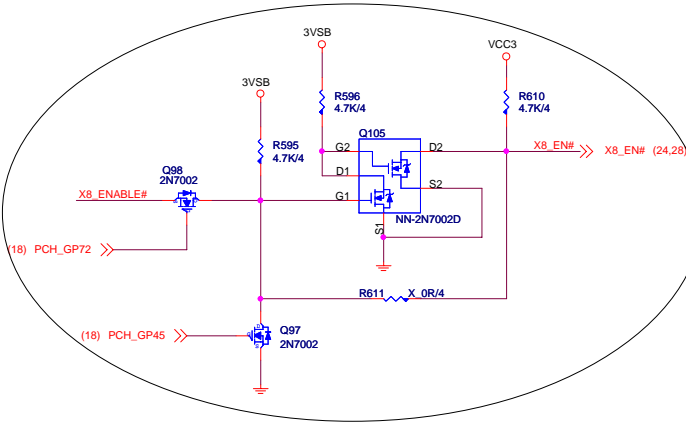


GPIO72

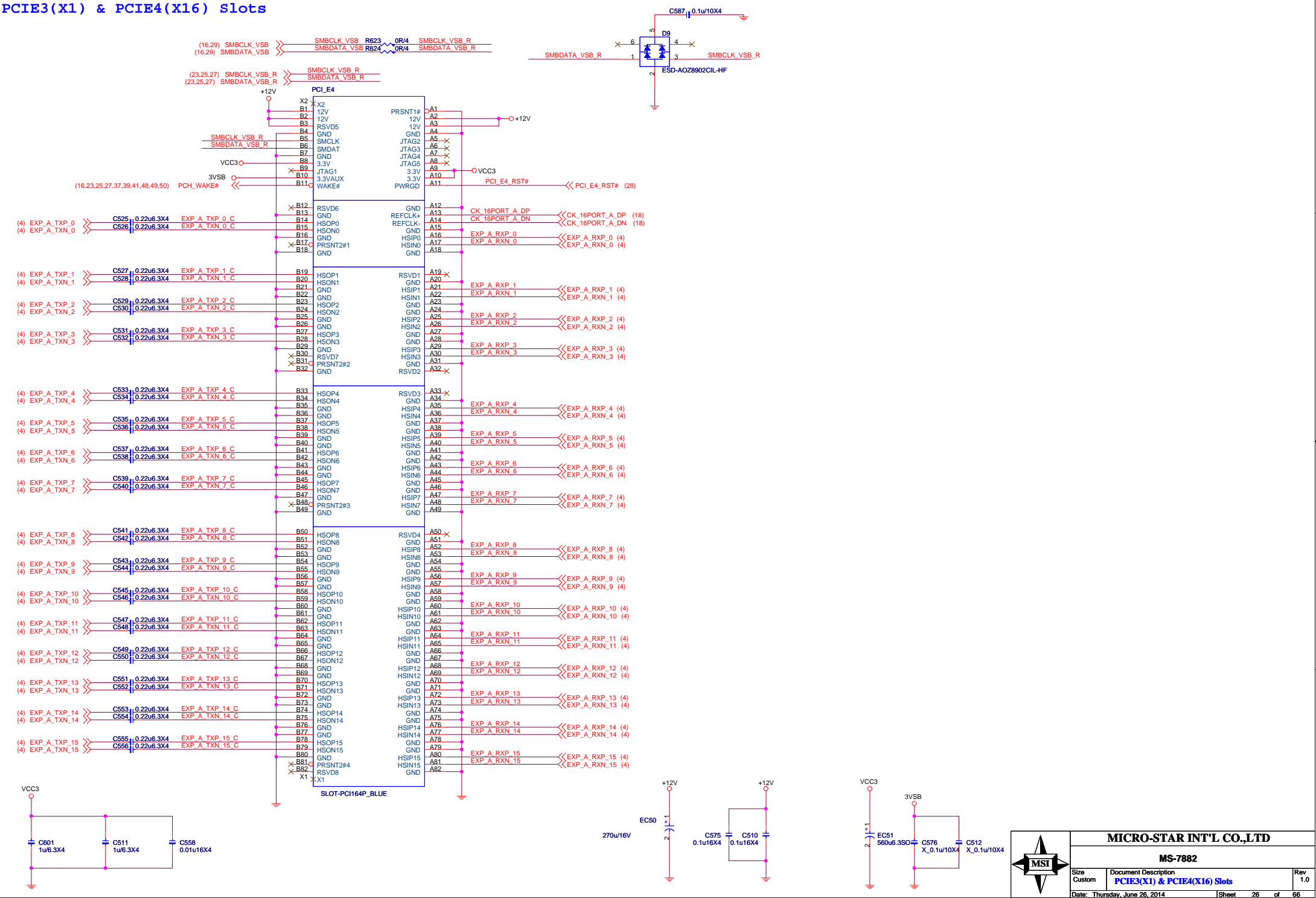
- 0: BIOS MODE
- 1: HW MODE

If USE HW MODE
PCH_GPIO45/47 programming to GPI
PCH_GPIO72 programming GPO
If USE BIOS MODE
PCH_GPIO45/47 programming to GPO

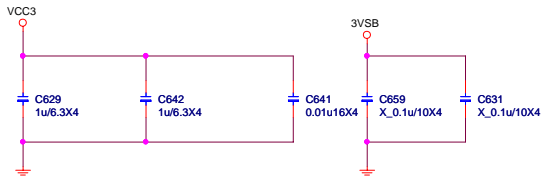
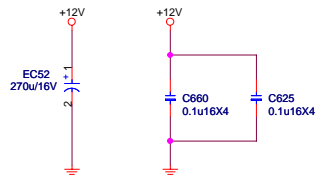
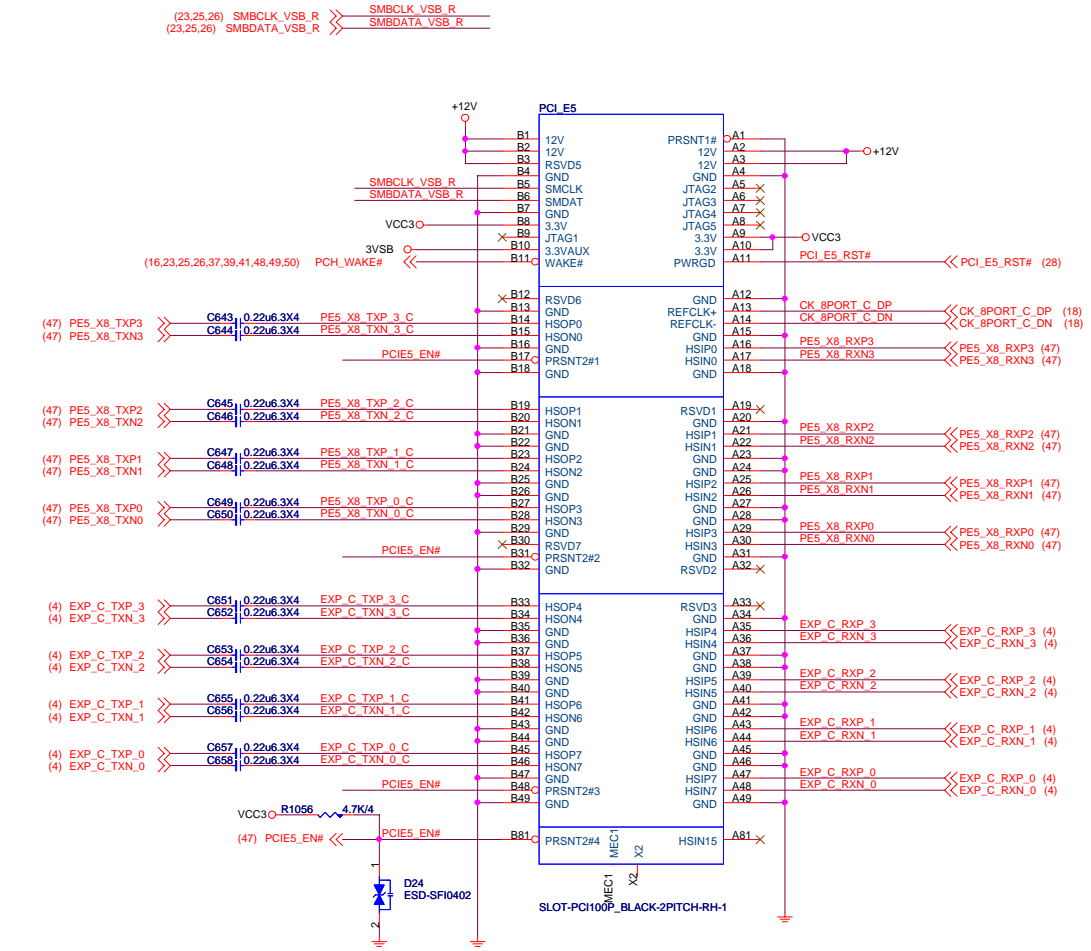
PCH Status	GPIO72	GPIO45	GPIO47
AUTO	1	GPI(def:0)	
16,0,0	0	X	X
8,8,0	0	1	0
8,0,8	0	0	1



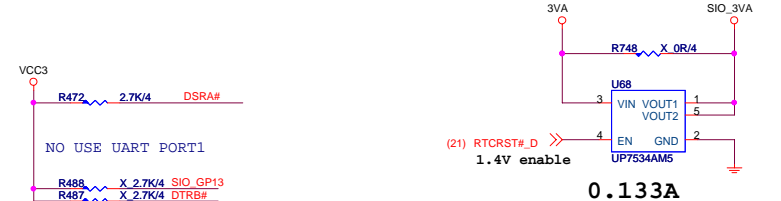
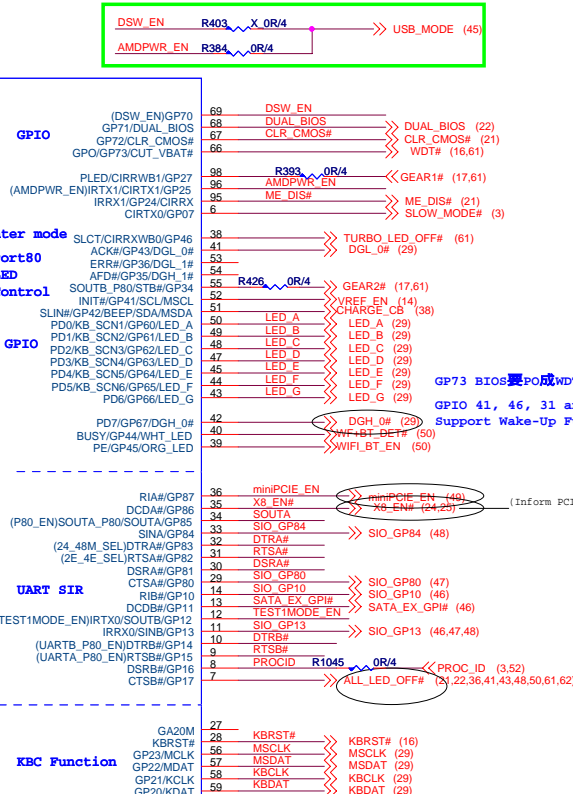
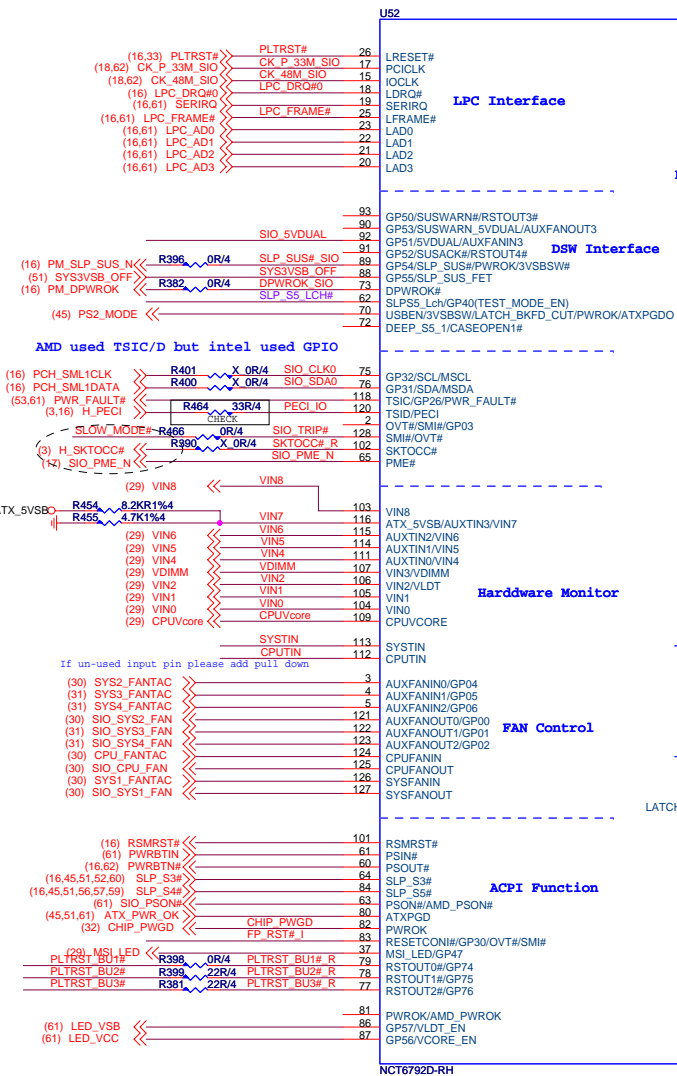
PCIE3(X1) & PCIE4(X16) Slots



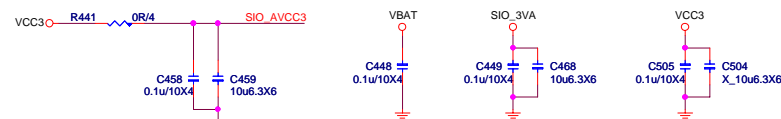
PCIE5(X8) Slots



SIO-NTC6792D/PS2



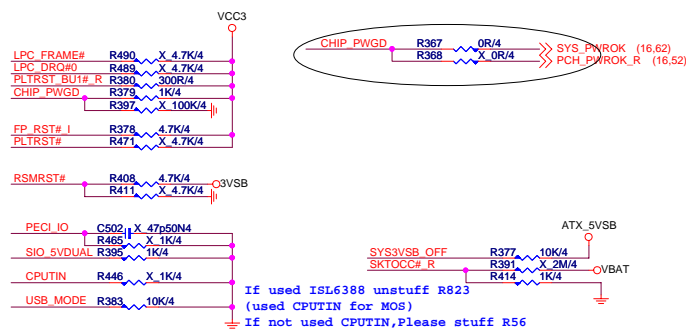
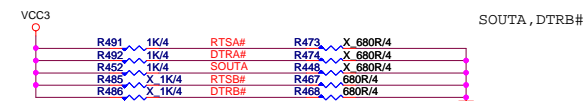
3V Analog Power



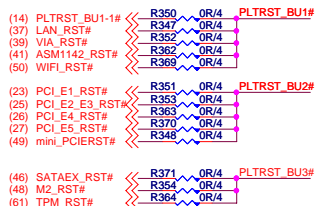
POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

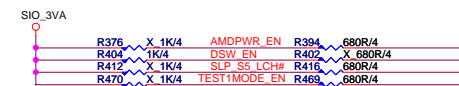
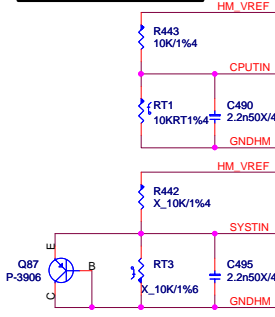
Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO



PLTRST Damping R



thermal senser



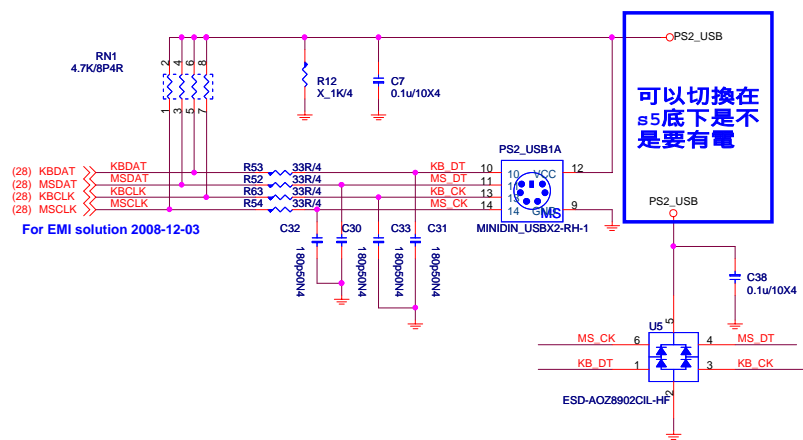
MICRO-STAR INT'L CO.,LTD

MS-7882

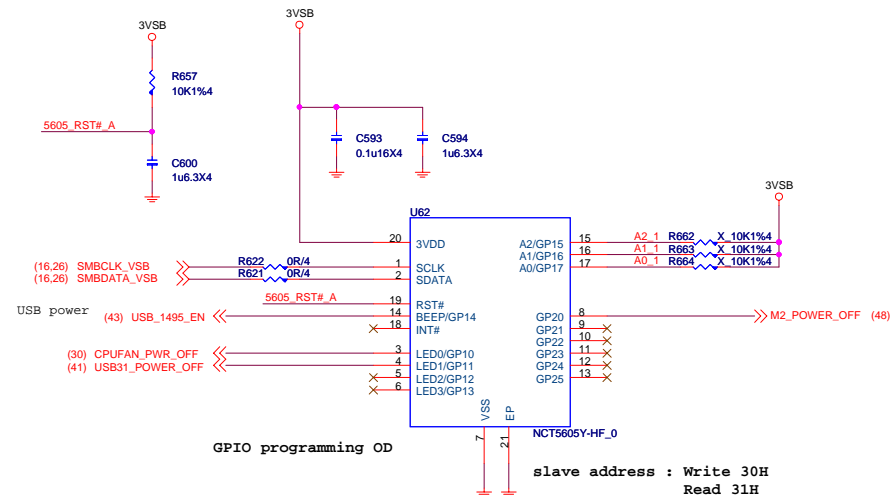
ent Description

Date: Thursday, June 26, 2014	Sheet 28 of 66
-------------------------------	----------------

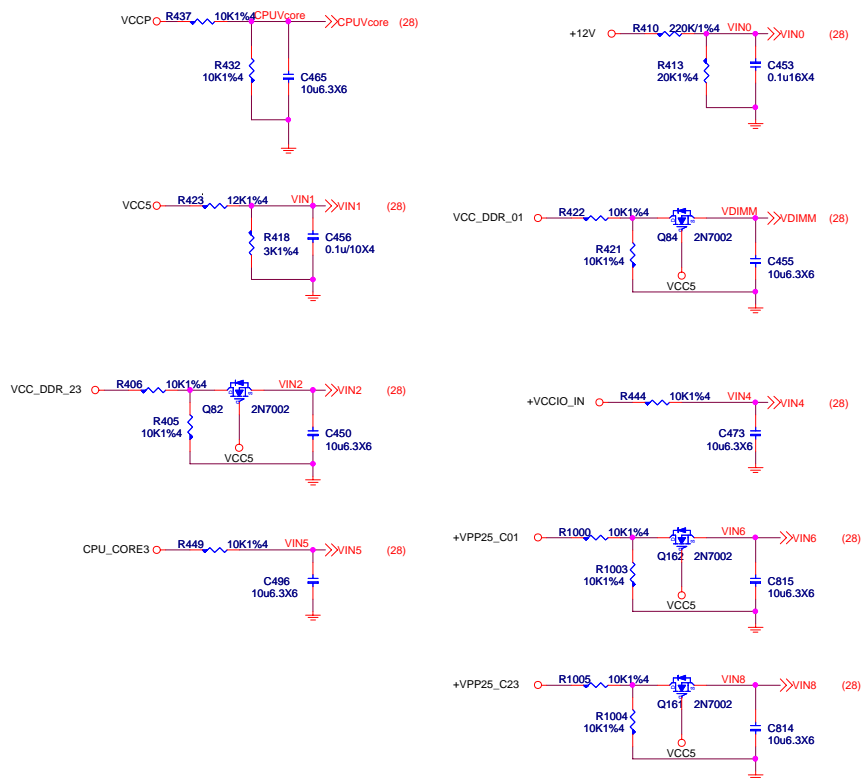
PS2 KEYBOARD & MOUSE CONNECTOR



CUT POWER CHIP

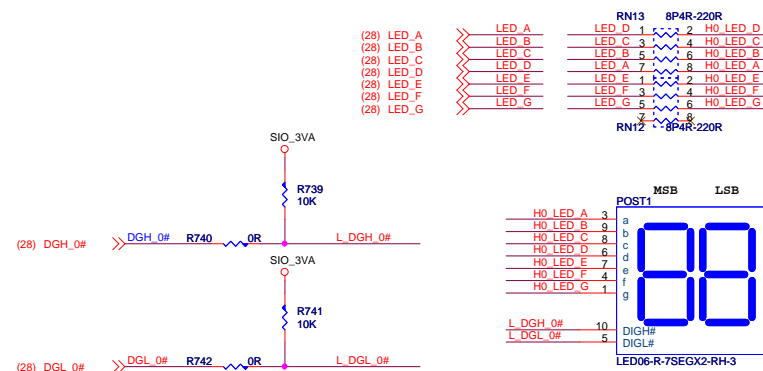


HW Monitor - Voltage

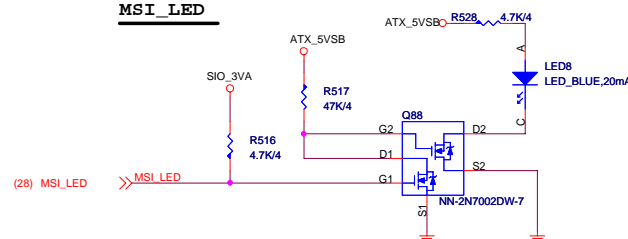


DEBUG LED

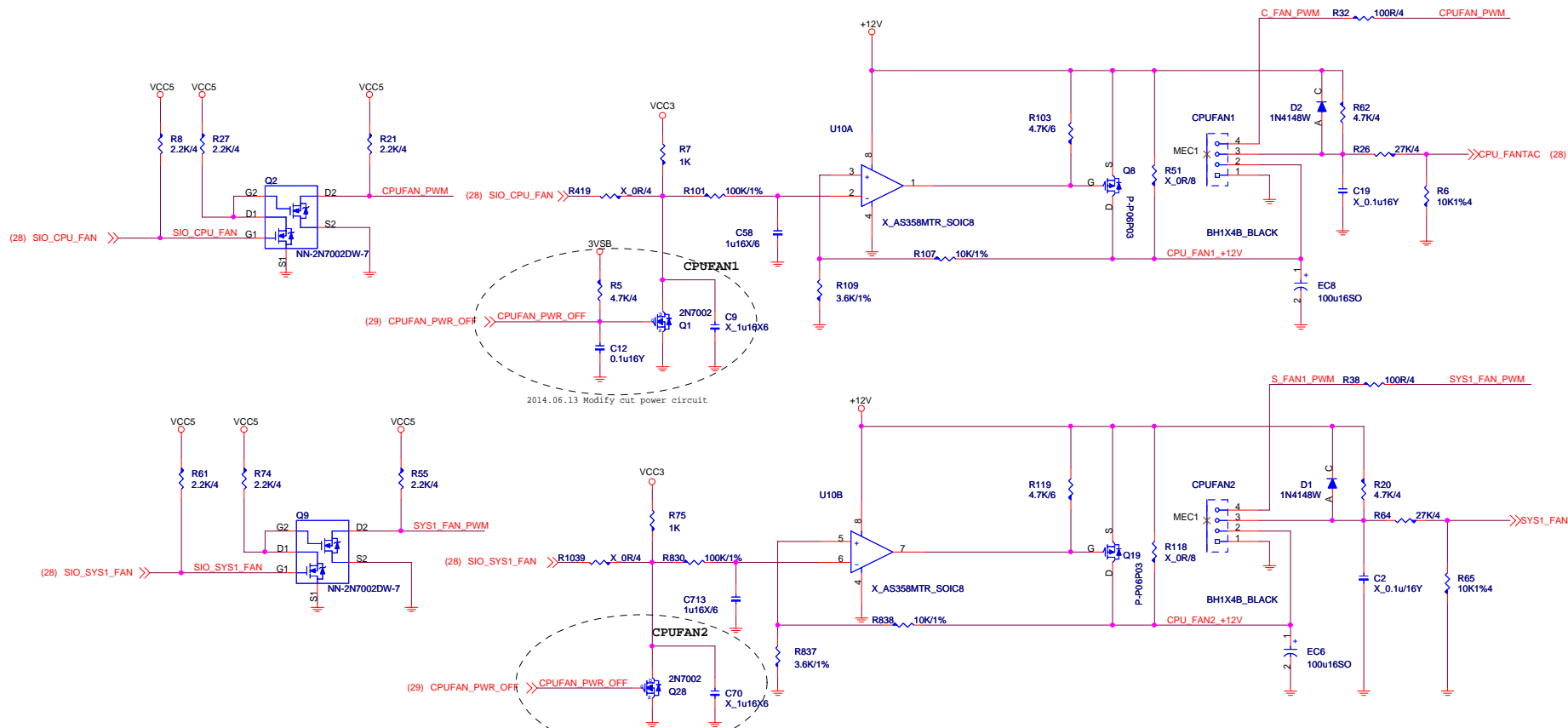
Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)



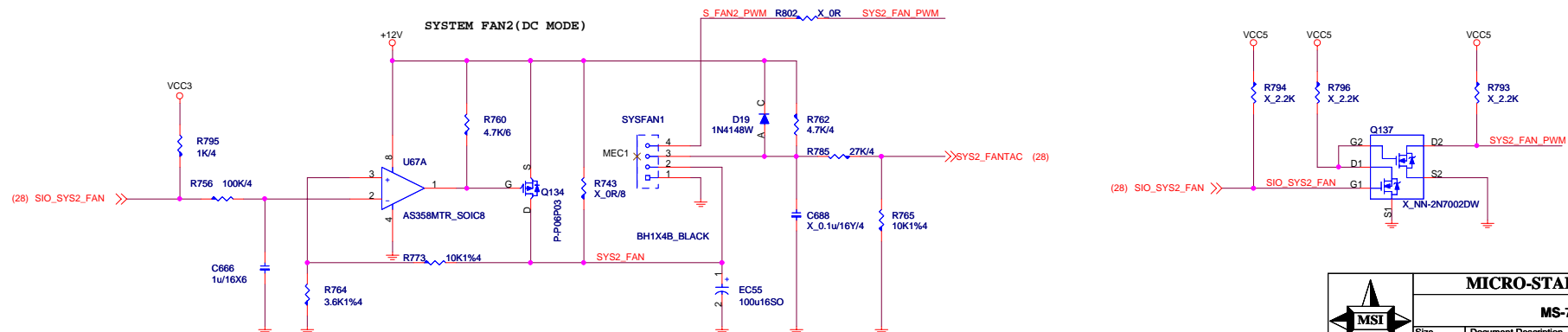
MSI_LED



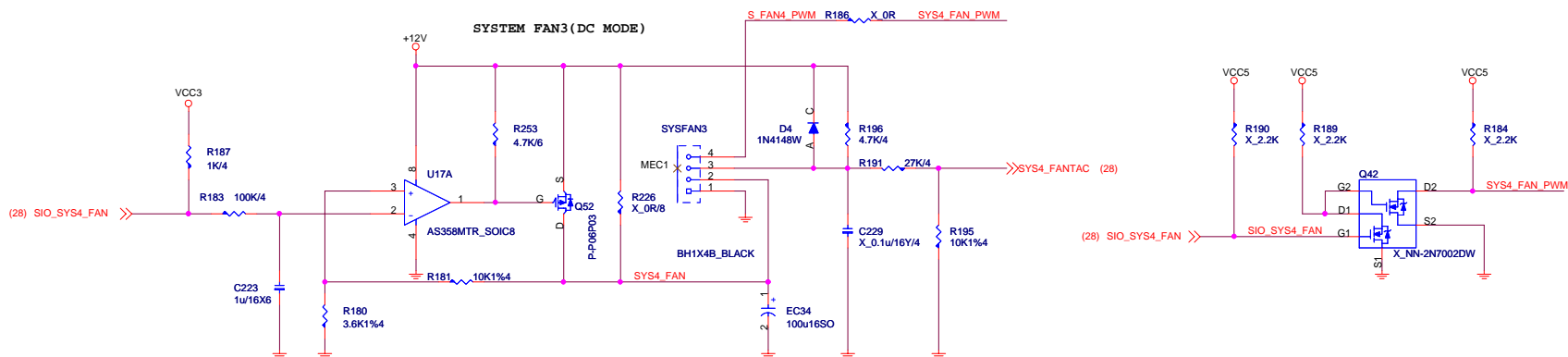
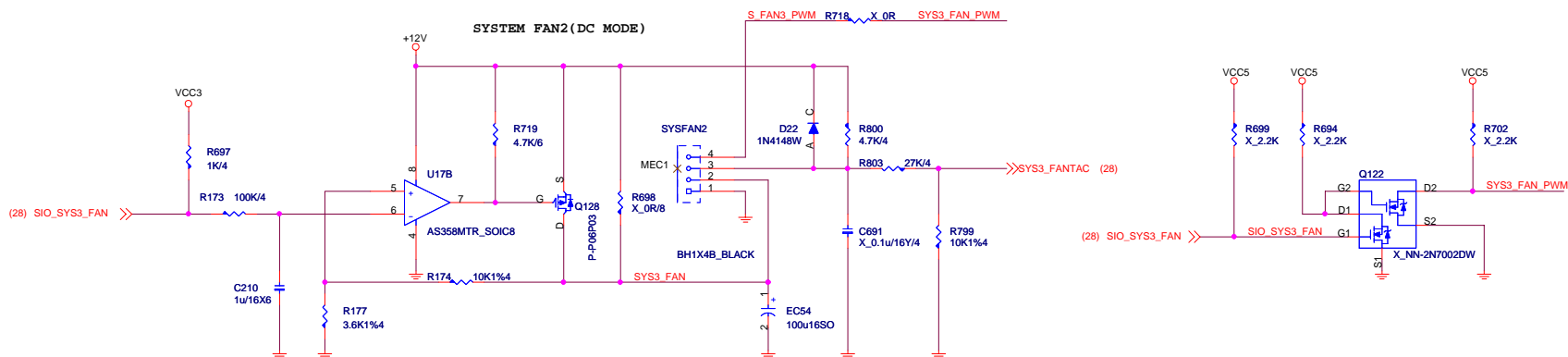
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE) (FOR NCT6792)



Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE) (FOR NCT6792)



Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)



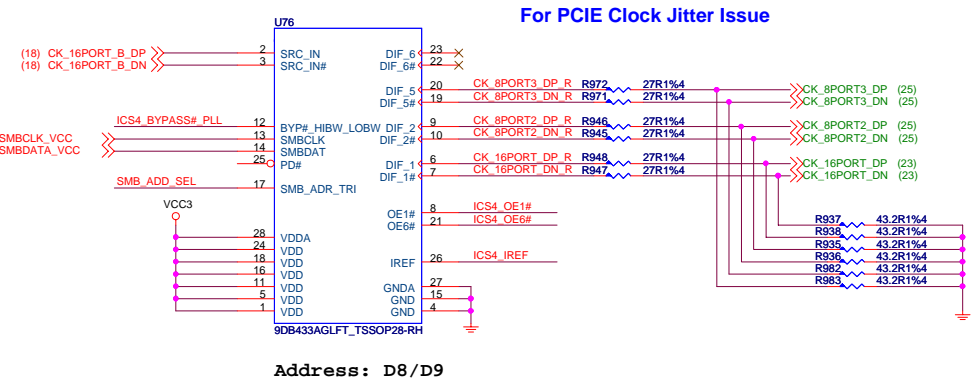
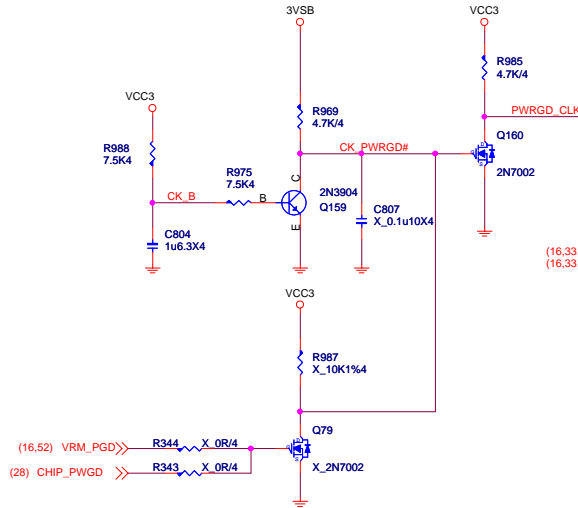
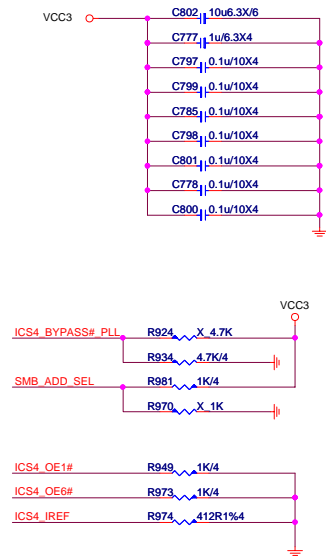
MICRO-STAR INT'L CO.,LTD

MS-7882

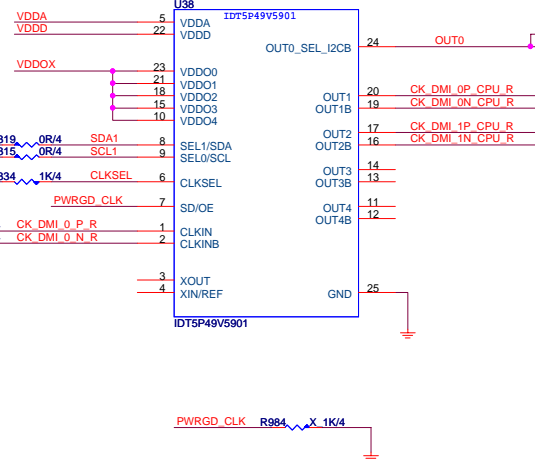
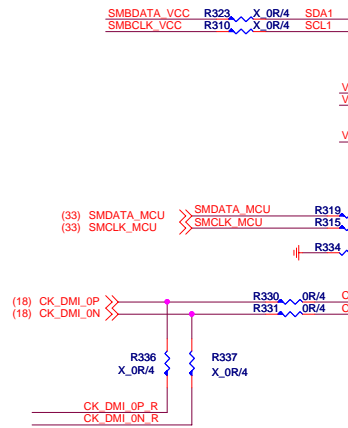
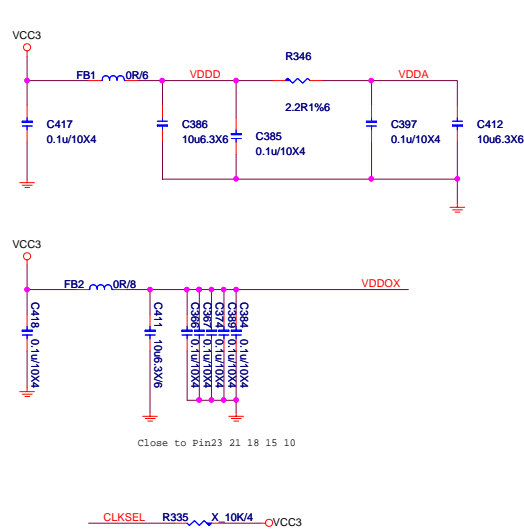
Size Custom	Document Description FAN CONTROLLOR-2	Rev 1.0
Date: Thursday, June 26, 2014		Sheet 31 of 66

Rev
1.0

CLK Buffer_9DB433

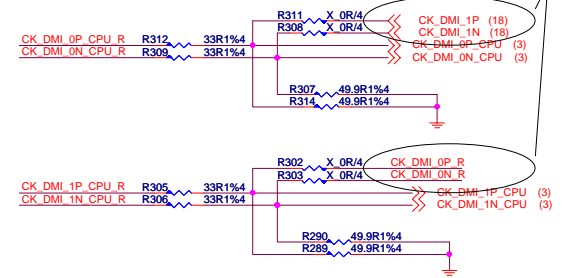


CLK GEN-IDT5P49V5901



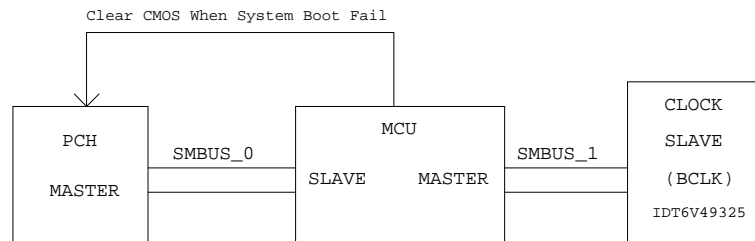
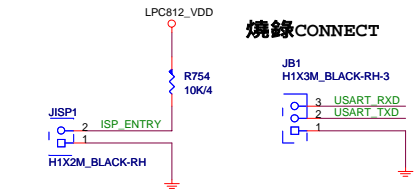
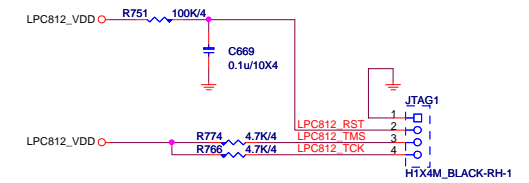
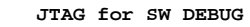
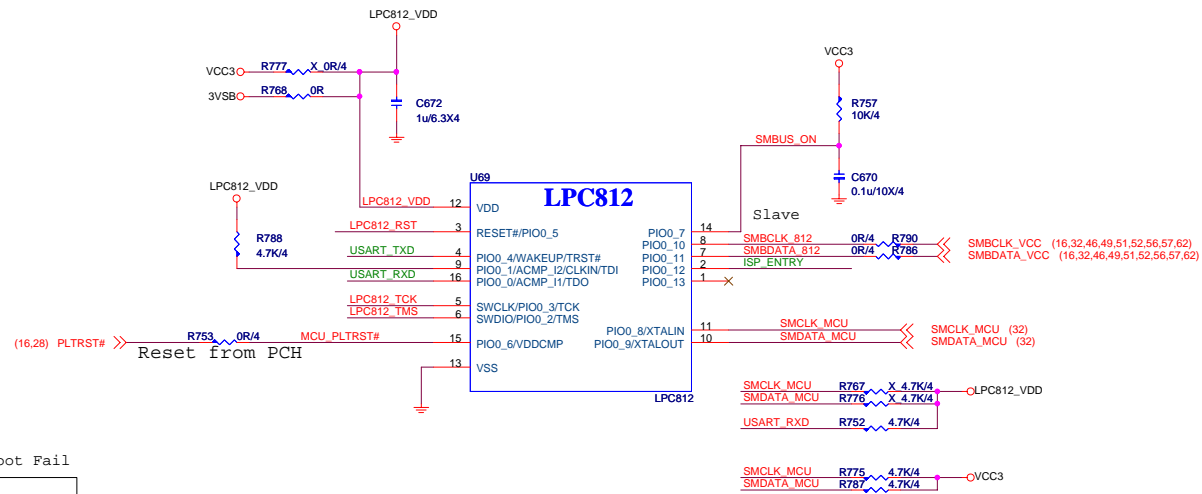
DMI0-to-BCLK1 have the shorter route length compared to DMI1-to-BCLK0

DMI1-to-BCLK0 pair and DMI0-to-BCLK1

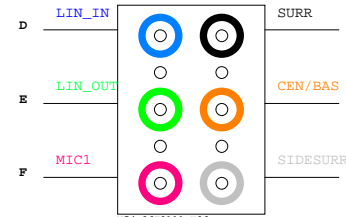
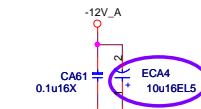
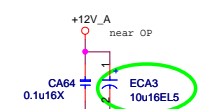
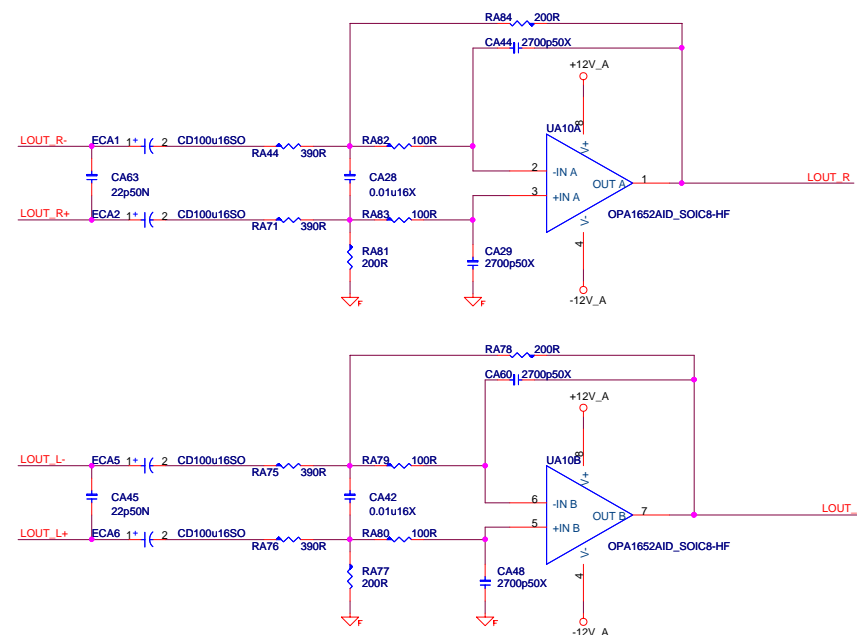
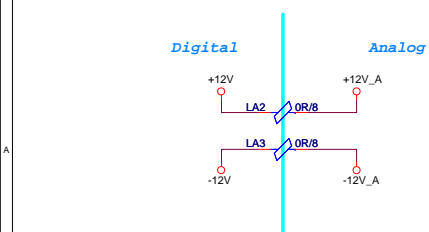
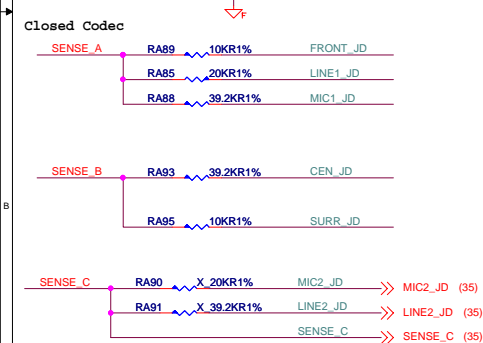
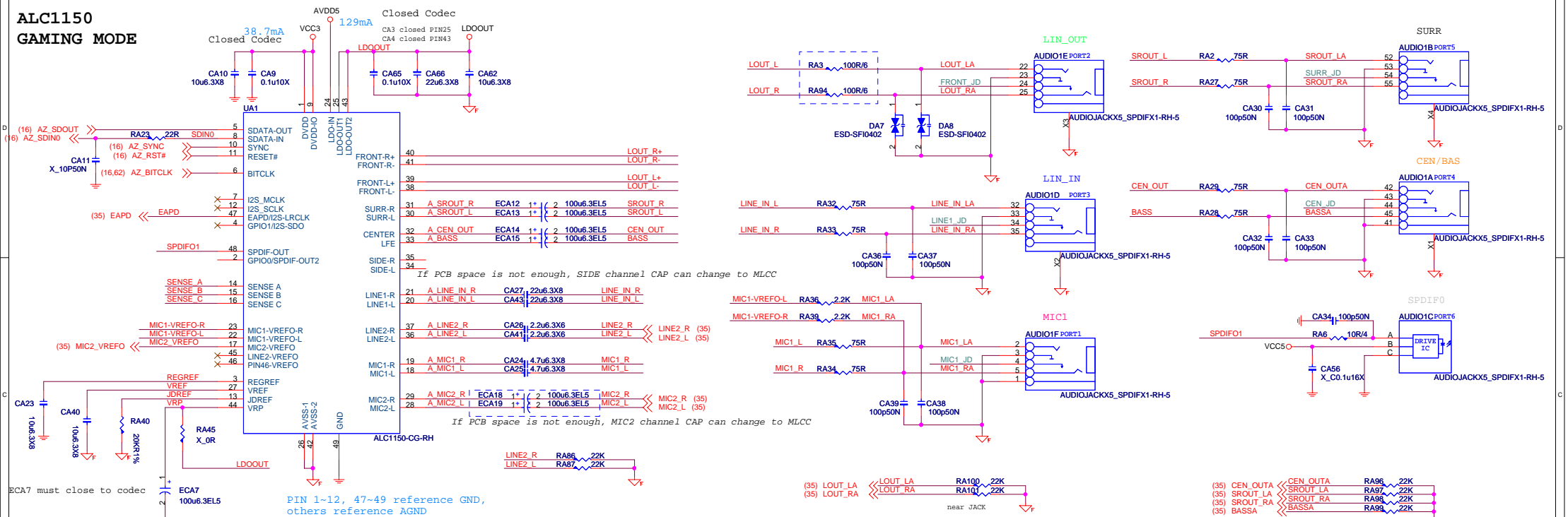


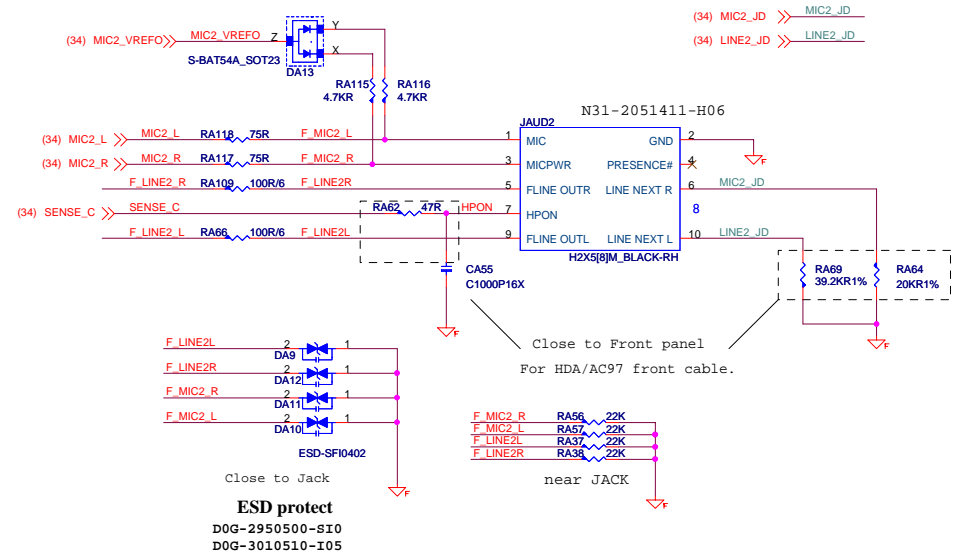
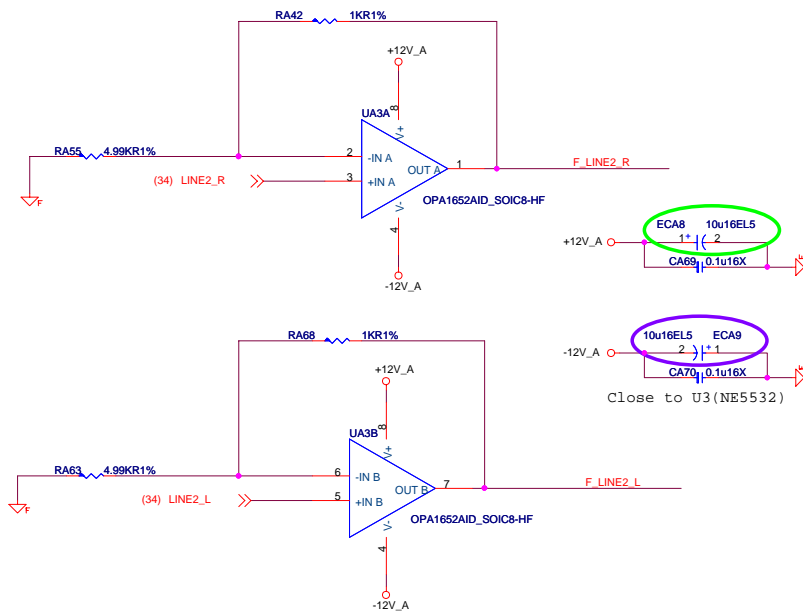
PIN:CLKSEL. Input clock select. Selects the active input reference source in manual switchover mode.
0 = XIN/REF, XOUT (default)
1 = CLKIN, CLKINB

SIO 6792 , GPIO13
default low , active high

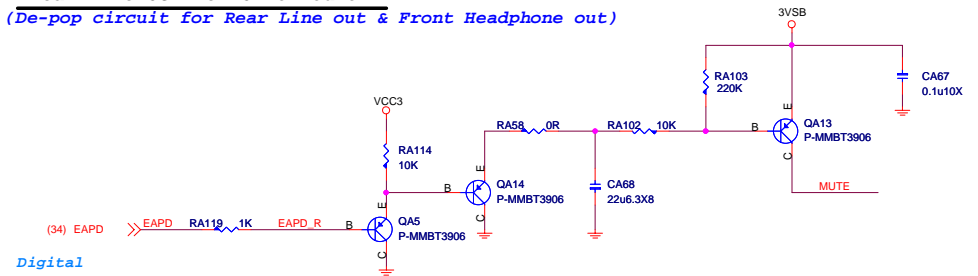


ALC1150
GAMING MODE

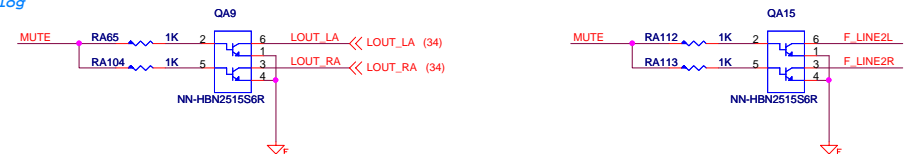




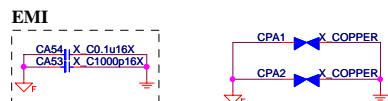
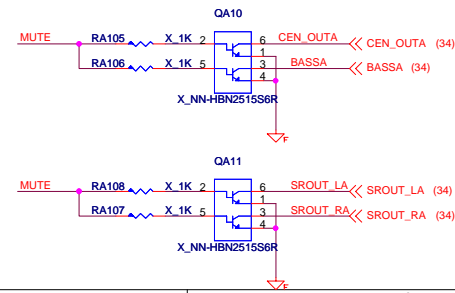
Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

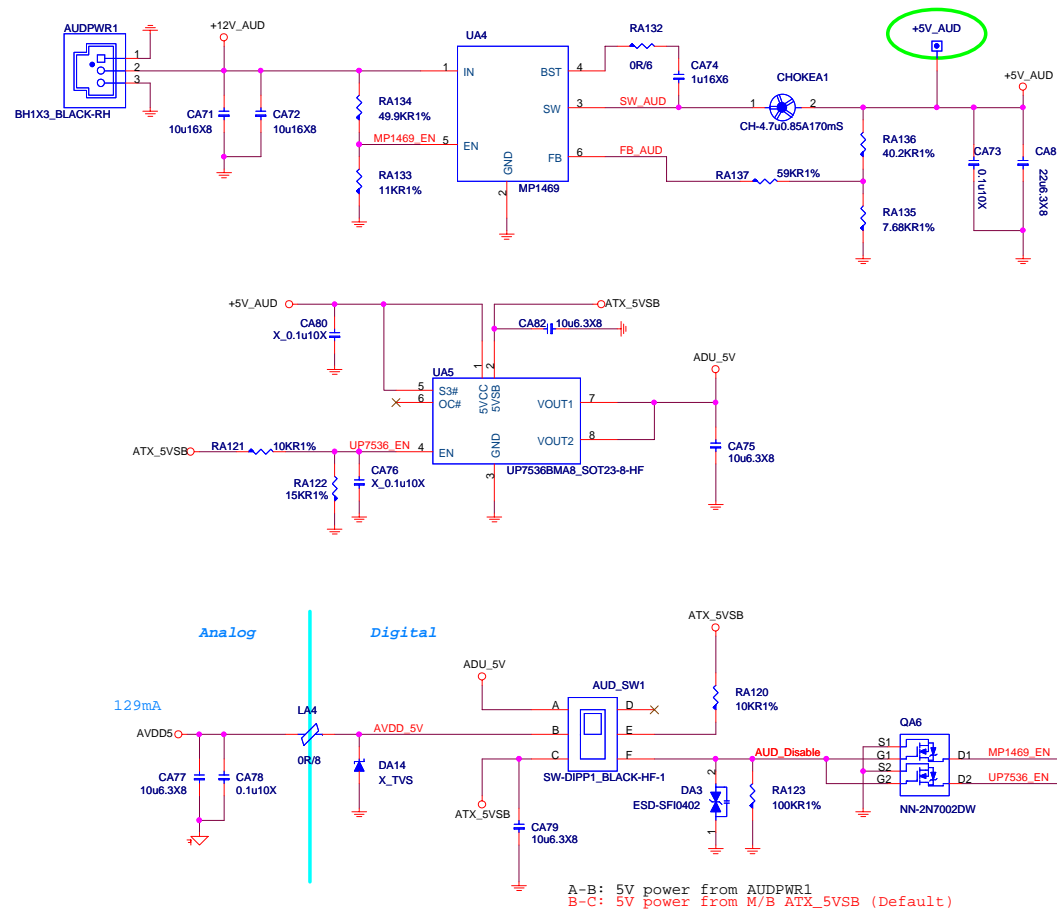


Analog



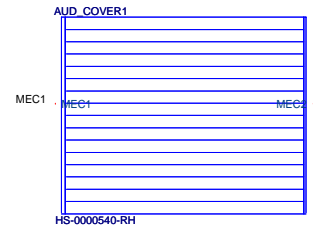
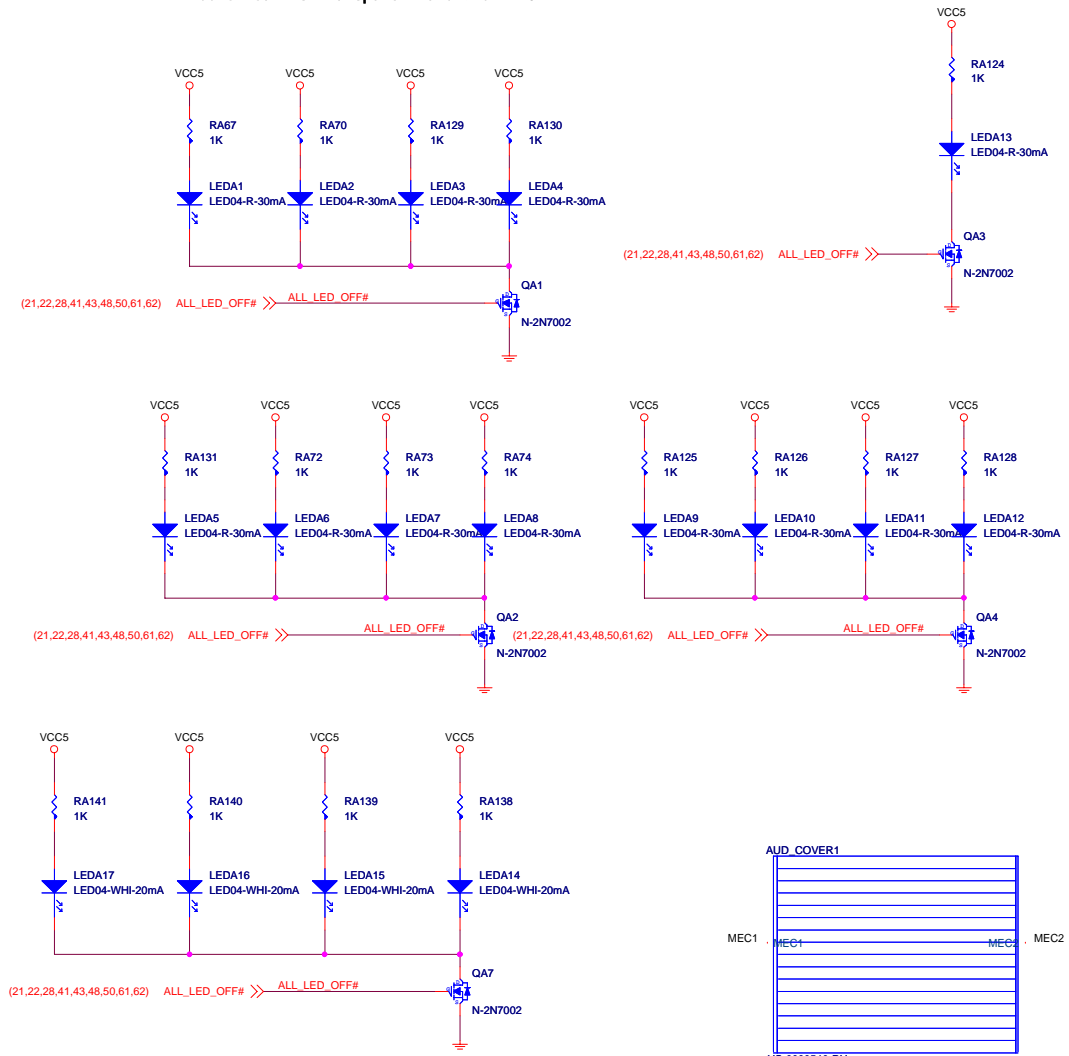
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA23, CA24 to TVS)



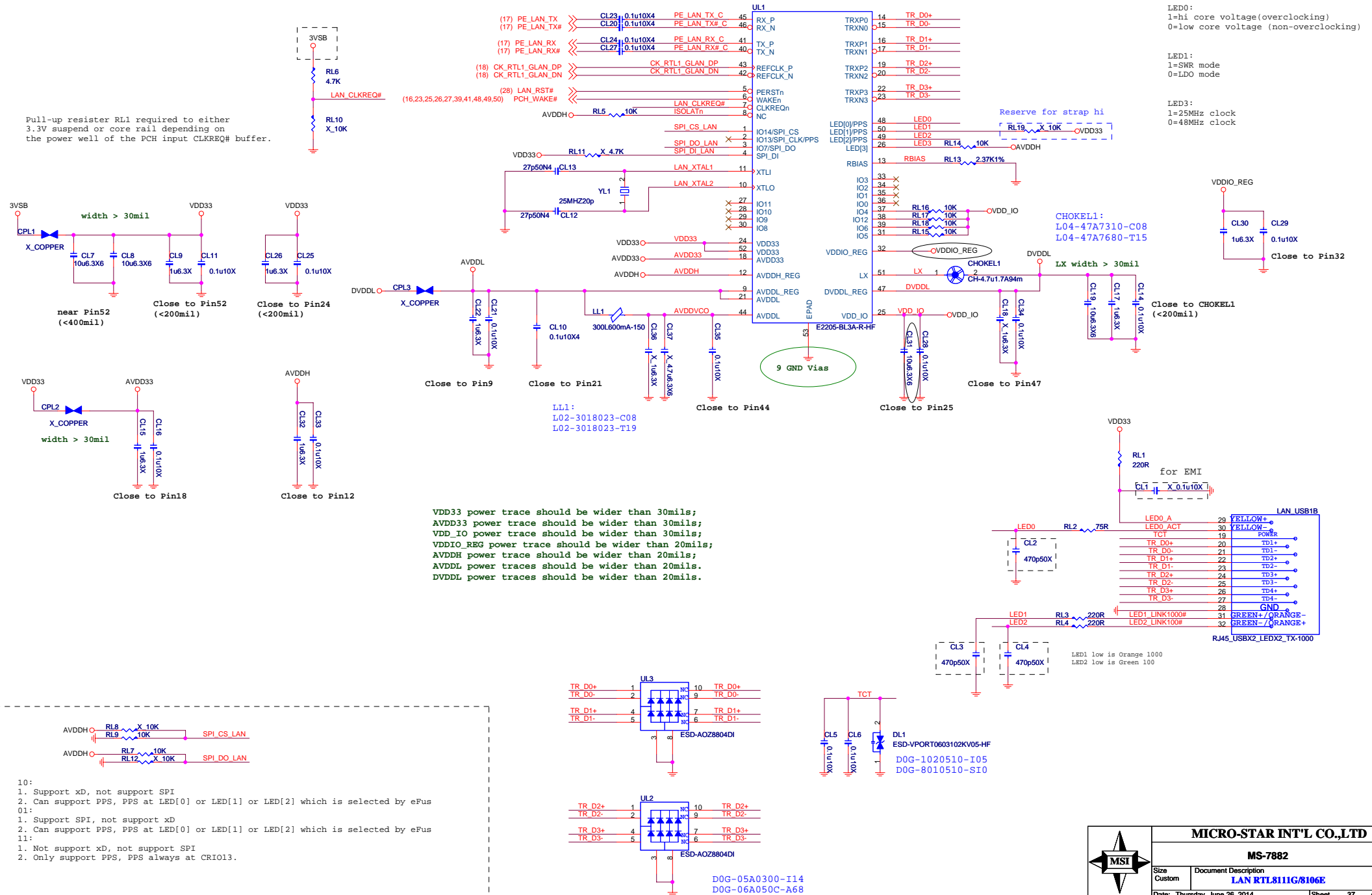


A-B: 5V power from AUDPWR1
B-C: 5V power from M/B ATX_5VSB (Default)

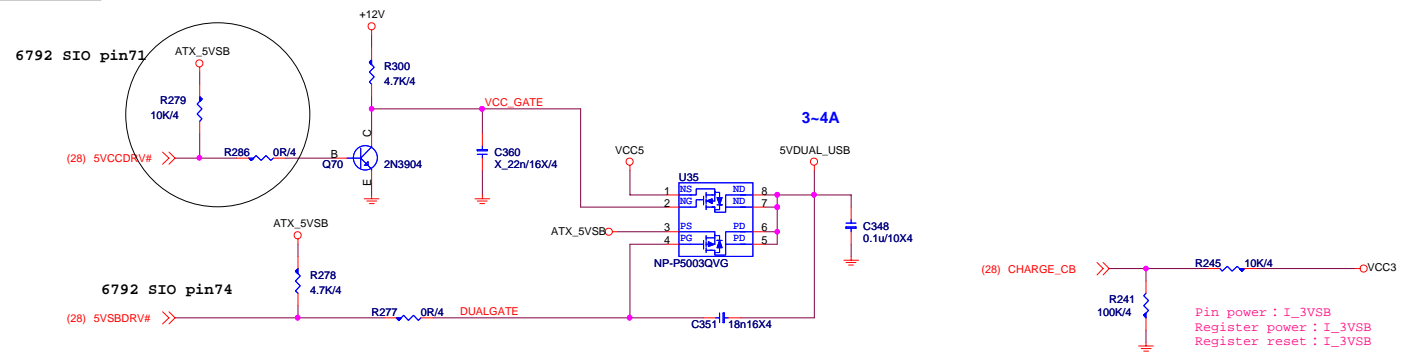
Audio moat is transparent and width 40mil



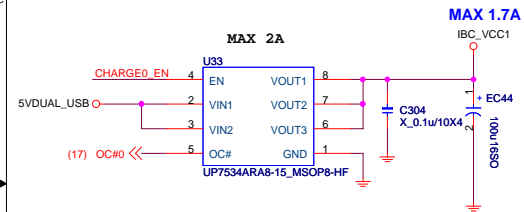
E2205-B Giga LAN



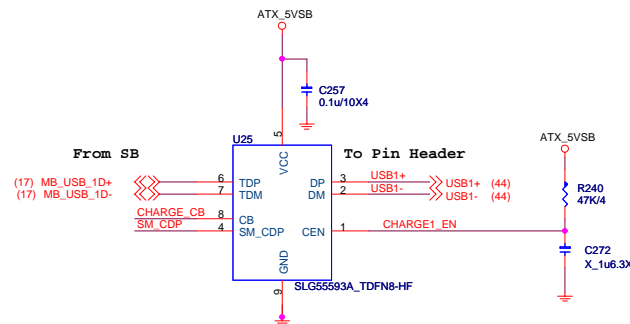
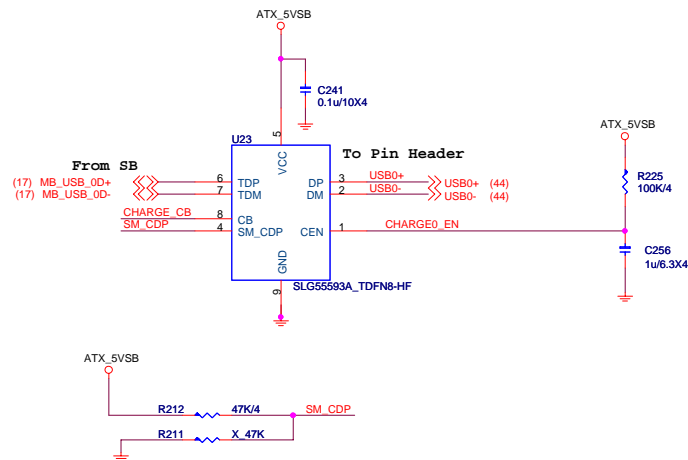
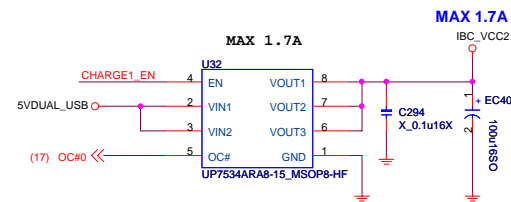
5VDUAL_USB



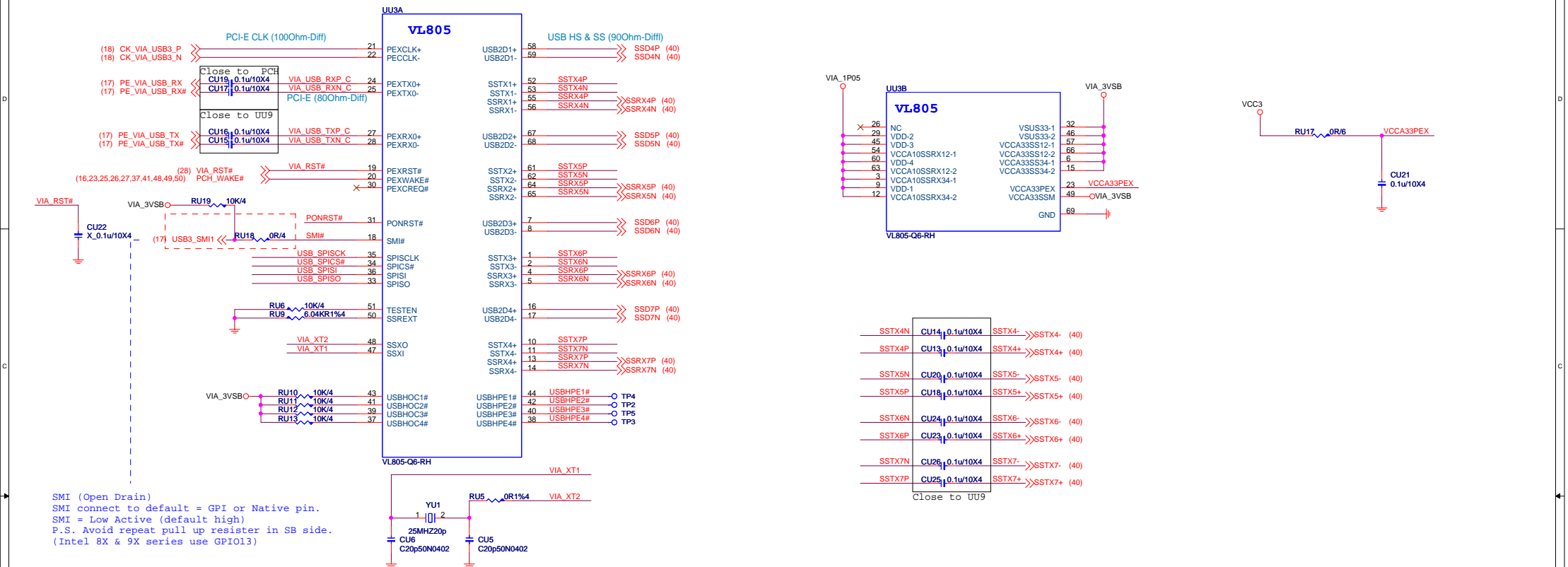
USB POWER PORT 0 For USB Charging



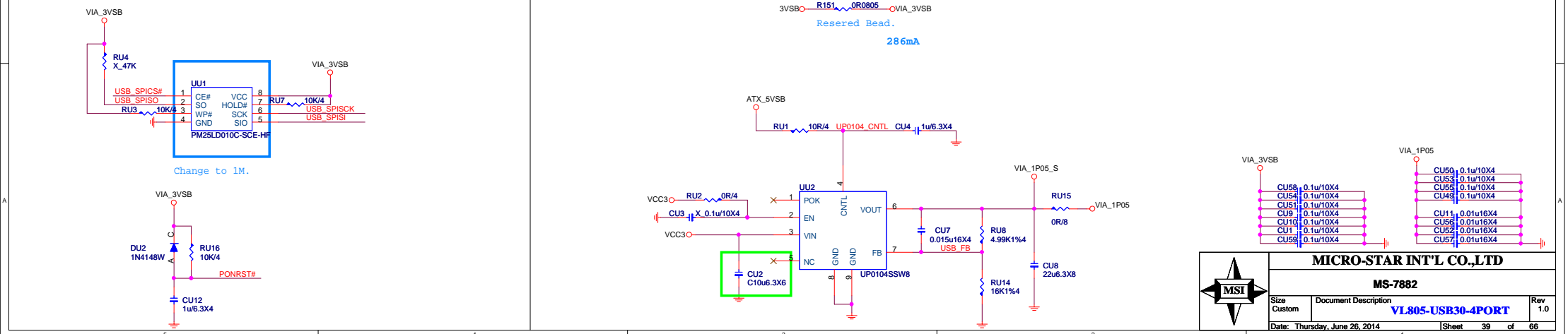
USB POWER PORT 1 For USB Charging

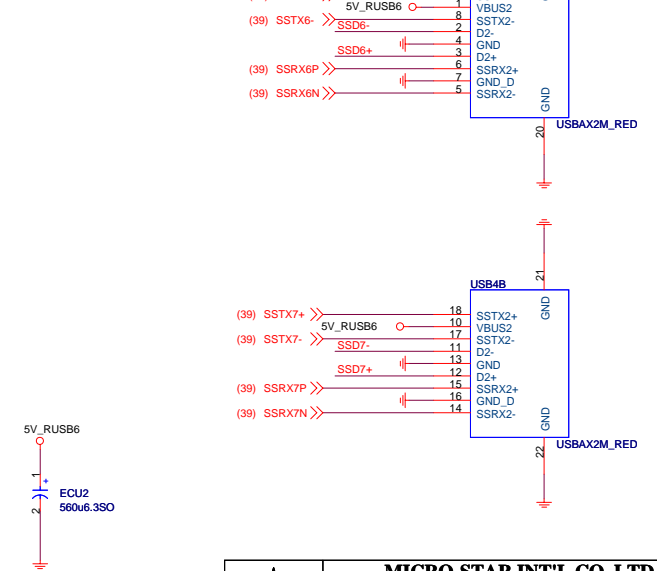
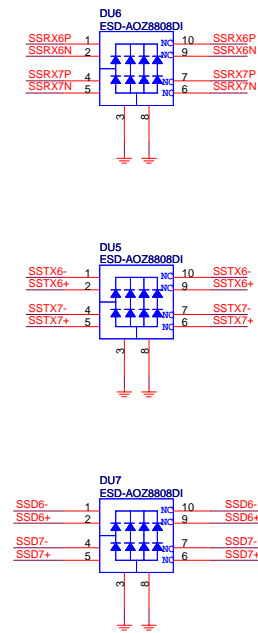
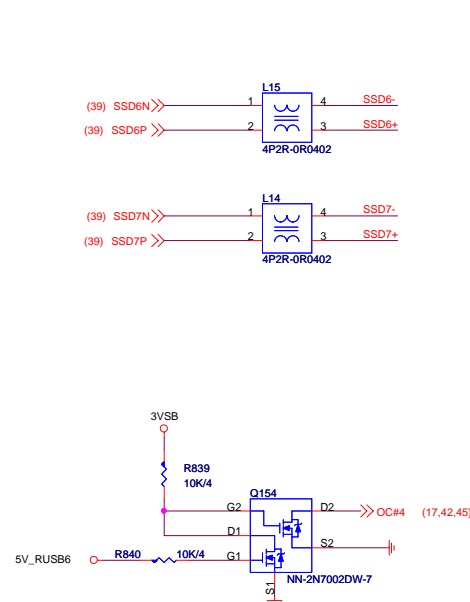
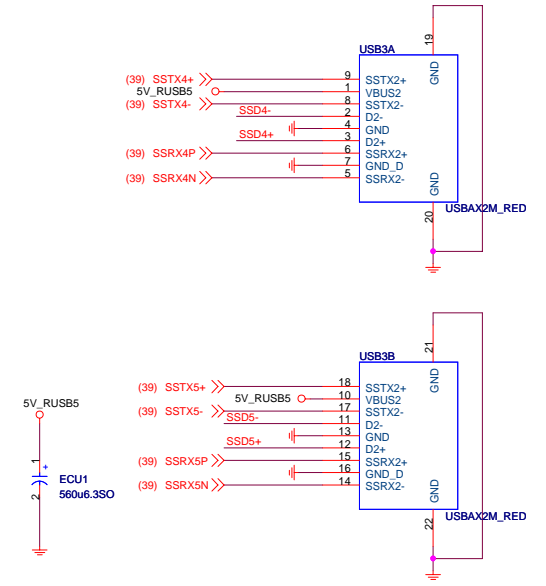
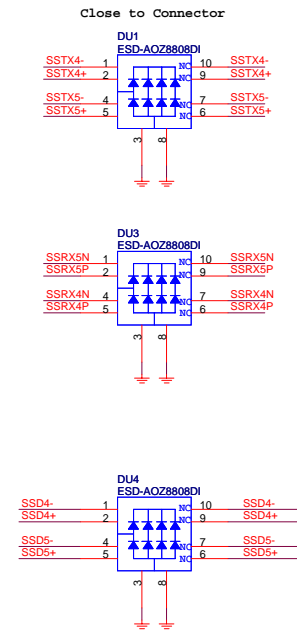
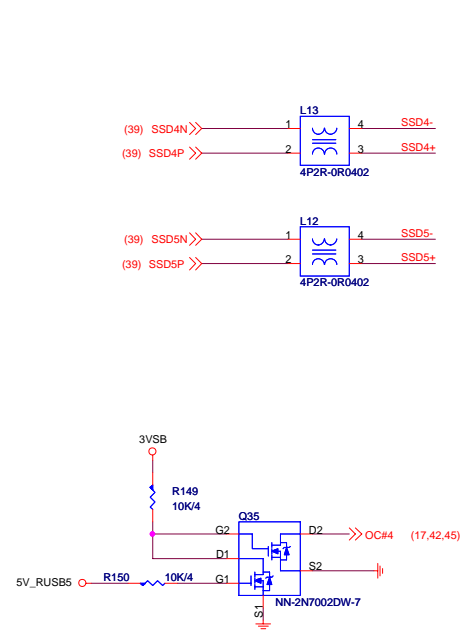


VL805-USB30-4PORT

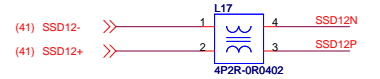


EEPROM



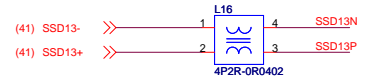


(41) SSTX12P >> SSTX12P CU37 0.22u6.3X4 SSTX12+
 (41) SSTX12N >> SSTX12N CU38 0.22u6.3X4 SSTX12-

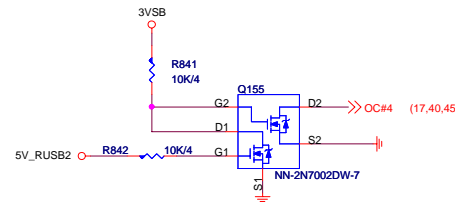


(41) SSRX12N >> SSRX12N
 (41) SSRX12P >> SSRX12P

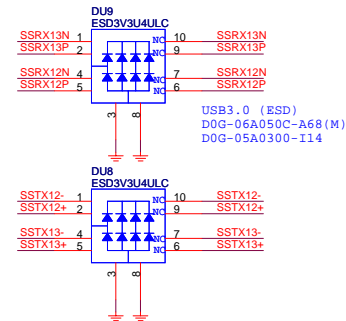
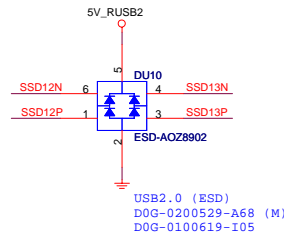
(41) SSTX13N >> SSTX13N CU35 0.22u6.3X4 SSTX13-
 (41) SSTX13P >> SSTX13P CU34 0.22u6.3X4 SSTX13+



(41) SSRX13N >> SSRX13N
 (41) SSRX13P >> SSRX13P

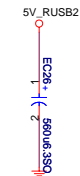
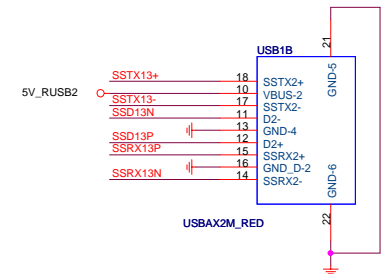
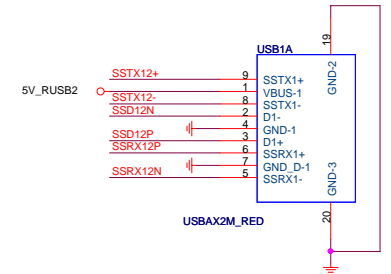


ESD Protection NEAR CONNECTOR



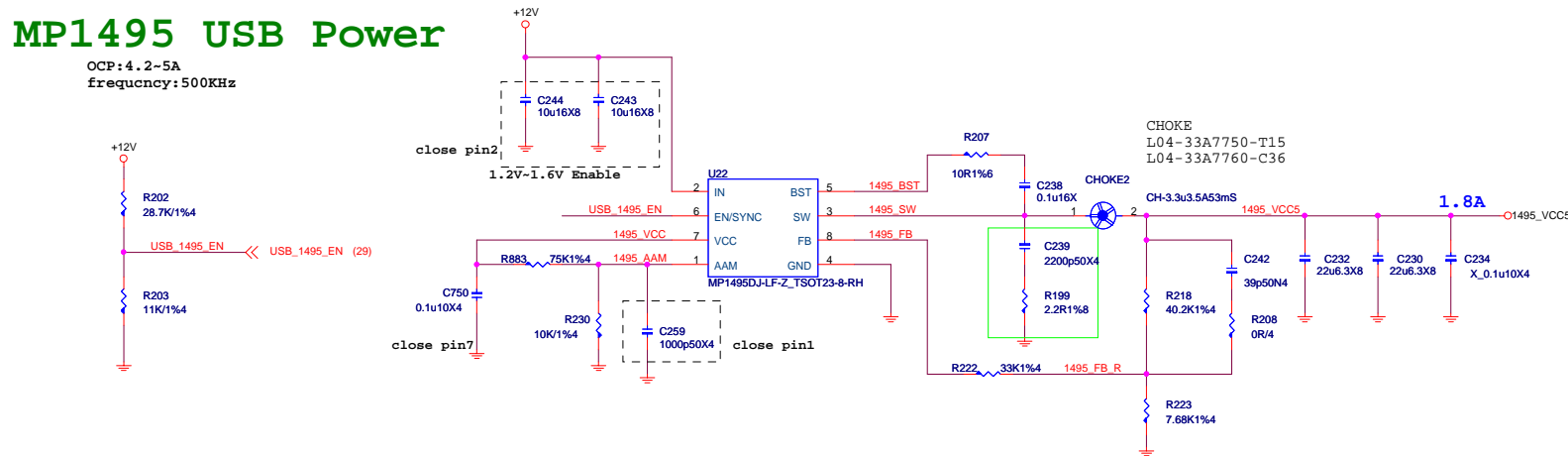
Rear USB3 CONN

Important--
 If USB3.0 signal connect to front pin header,
 please must less than 0.6 inch, short trace
 has better eye diagram with some bad fly cable by SI customer.



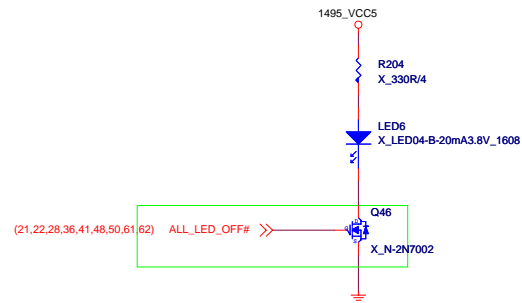
MP1495 USB Power

OCP:4.2-5A
frequency:500KHz

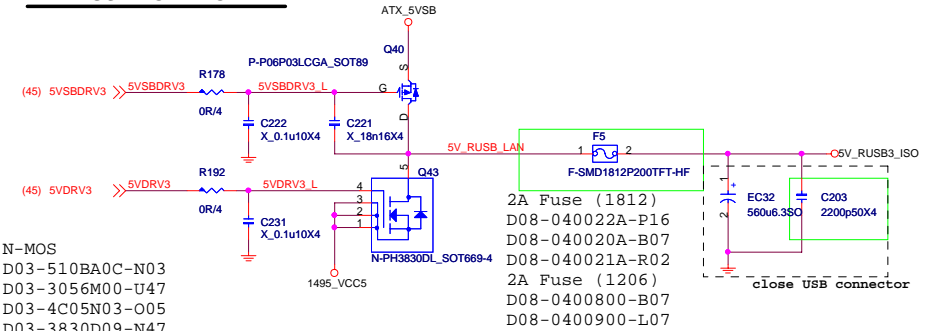


OC# signal connect to SB OC pin
OC# can not be shared with other usb

TO:NCT6792D GP17

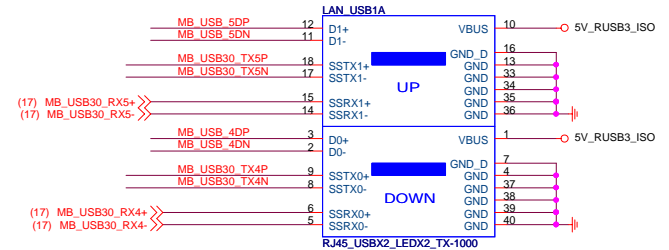
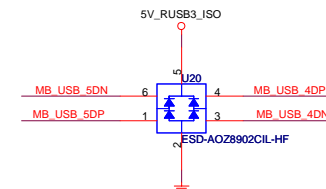


REAR USB PORT POWER



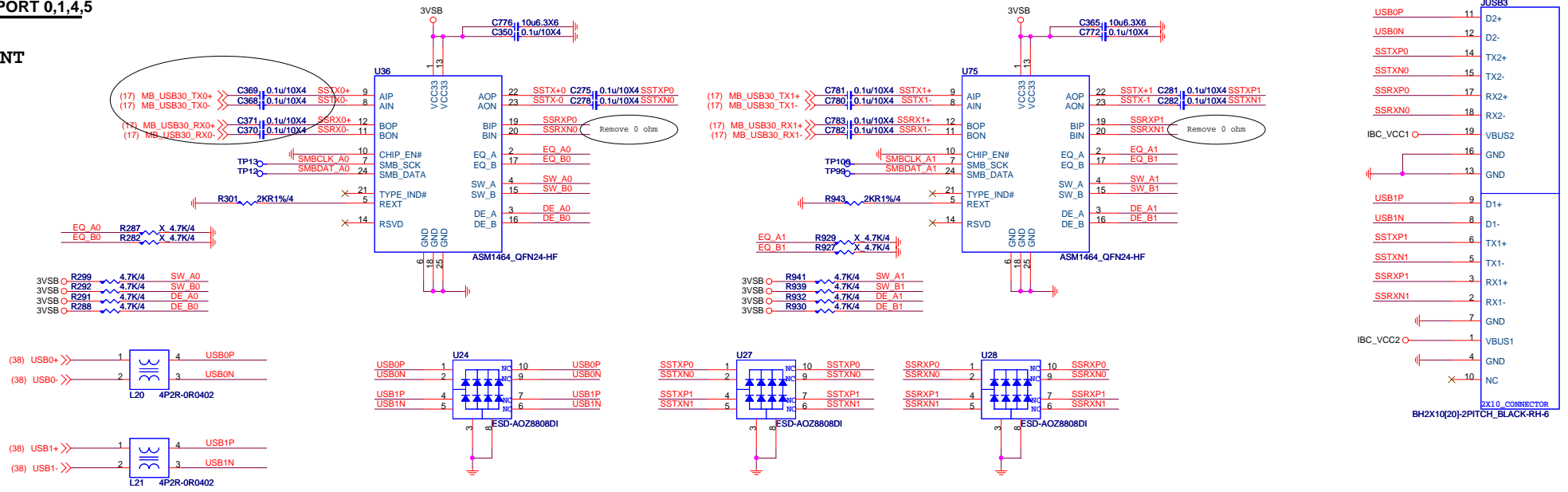
(D03-P500303-N03 N/P MOS can replace Q1/Q2)

USB3.0 Connector



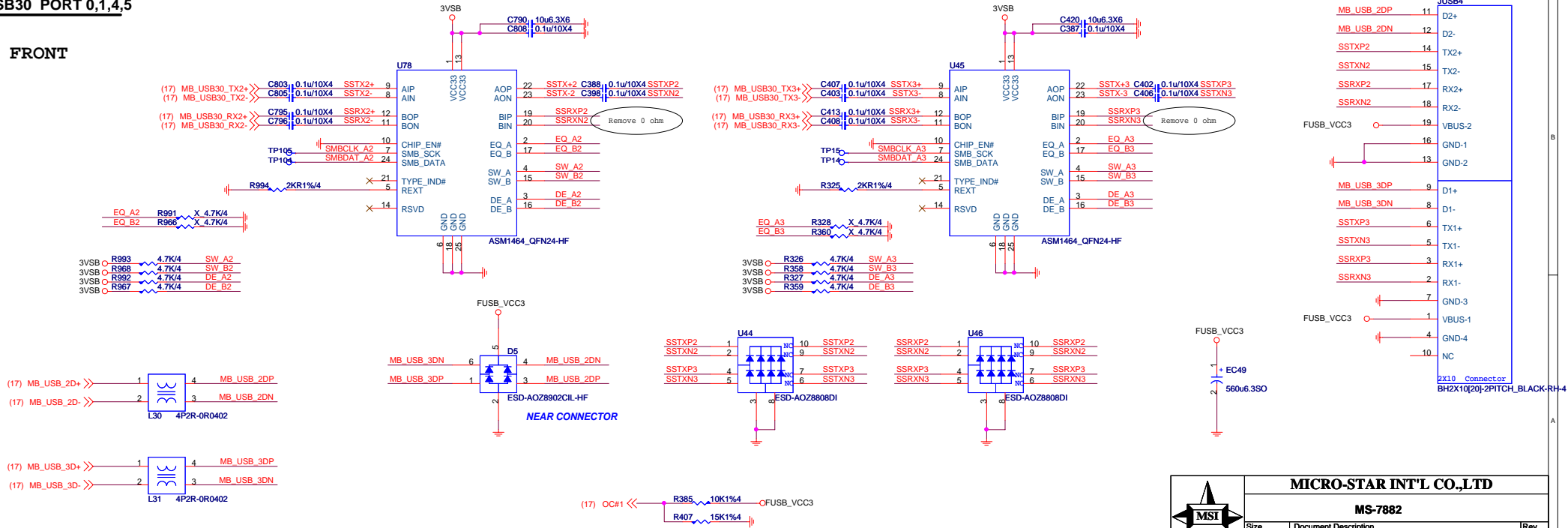
FRONT USB30 PORT 0,1,4,5

USB3.0 FRONT



FRONT USB30 PORT 0,1,4,5

USB3.0 FRONT

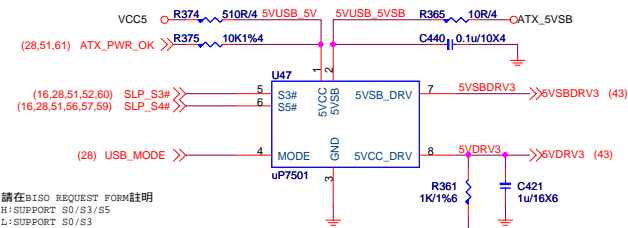


MICRO-STAR INT'L CO.,LTD

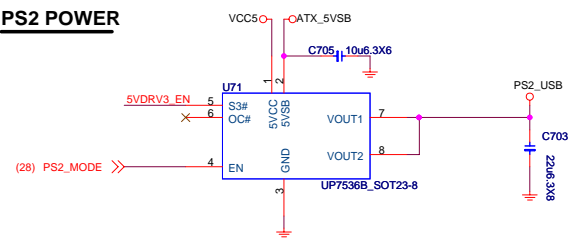
MS-7882

Size	Document Description	Rev
Custom	USB3.0 FRONT	1.0
Date: Thursday, June 26, 2014		Sheet 44 of 66

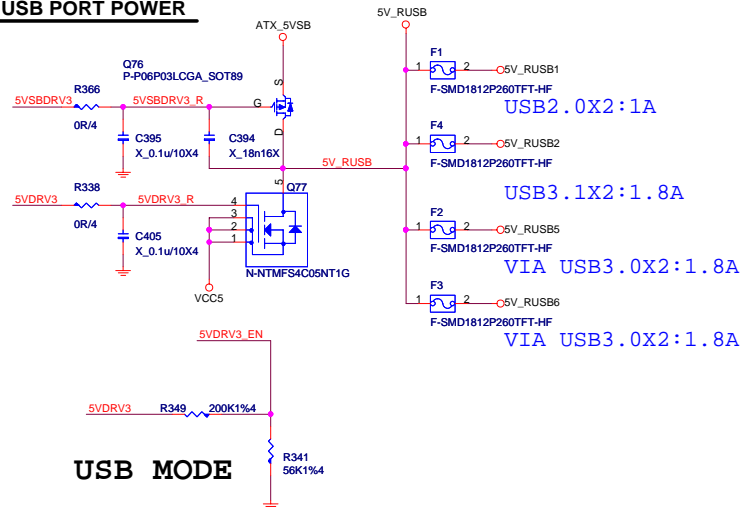
USB POWER



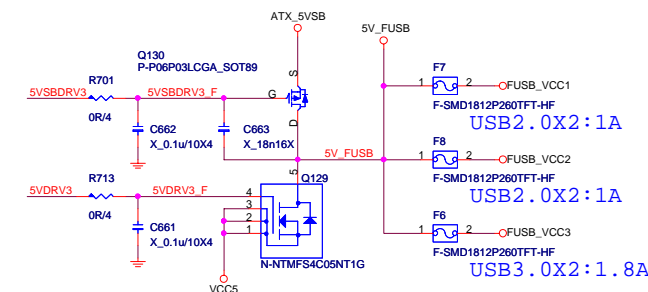
PS2 POWER



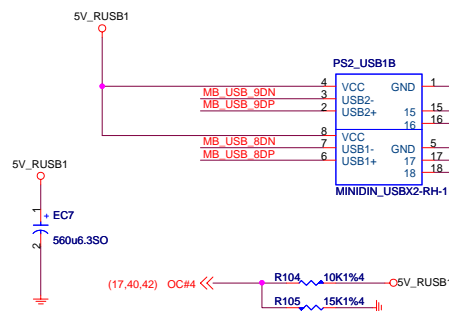
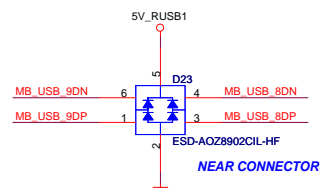
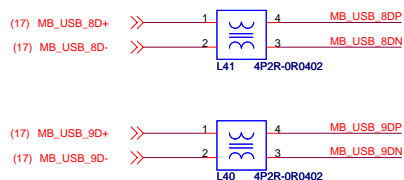
REAR USB PORT POWER



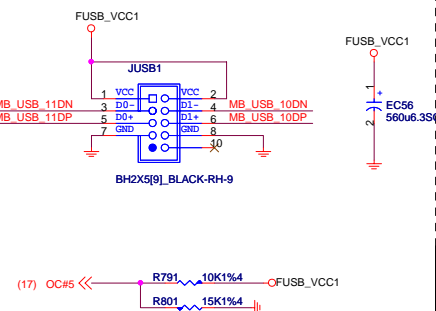
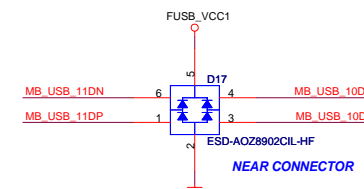
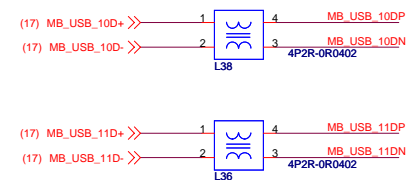
Front USB PORT POWER



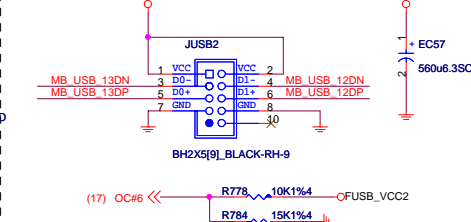
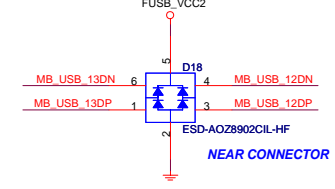
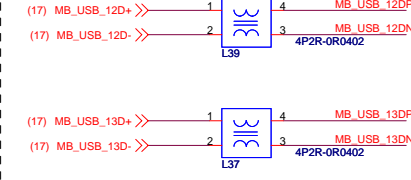
REAR USB PORT 8,9 (With PS2)



FRONT USB PORT 10,11



FRONT USB PORT 12,13



SATA 6G PORT 2.3

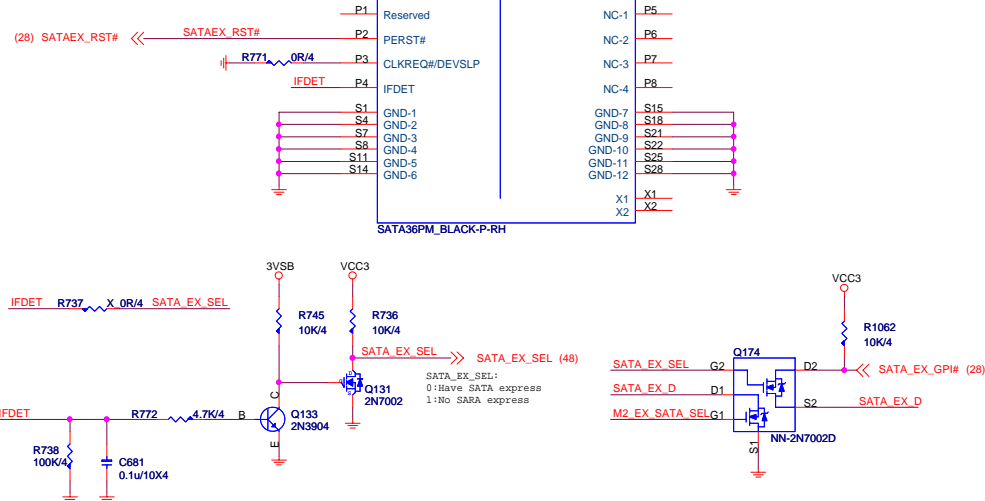
Pinout details for SATA 6G PORT 2.3:

- TX0 Signals:**
 - (17) SATA_TX0 ↔ C452 0.01u16X4 ST_TX0
 - (17) SATA_TX#0 ↔ C454 0.01u16X4 ST_TX#0
- RX#0 Signals:**
 - (17) SATA_RX#0 ↔ C450 0.01u16X4 ST_RX#0
 - (17) SATA_RX0 ↔ C493 0.01u16X4 ST_RX0
- Internal Connections:**
 - TX0 signals connect to S3HT#1, S3HT#2, S3HT#1, S3HT#2, S3HR#1, S3HR#2, S3HR#1, S3HR#2.
 - RX#0 signals connect to GND#2, GND#5, GND#3, GND#6.
 - TX#0 and RX0 signals connect to ST_TX#1, ST_TX#1, ST_RX#1, ST_RX#1.
 - TX#1 and RX#1 signals connect to C457, C464, C471, C472.
- MEC Connections:**
 - MEC1 connects to X1, X1, X2, X2.
 - MEC2 connects to X1, X1, X2, X2.
- Component Labels:**
 - SATA1_2
 - SATA14PM_BLACK-RH-2

[illegible]

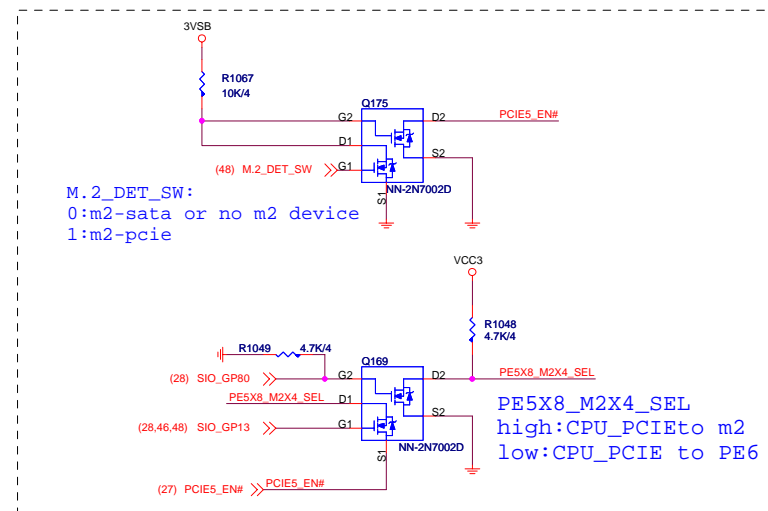
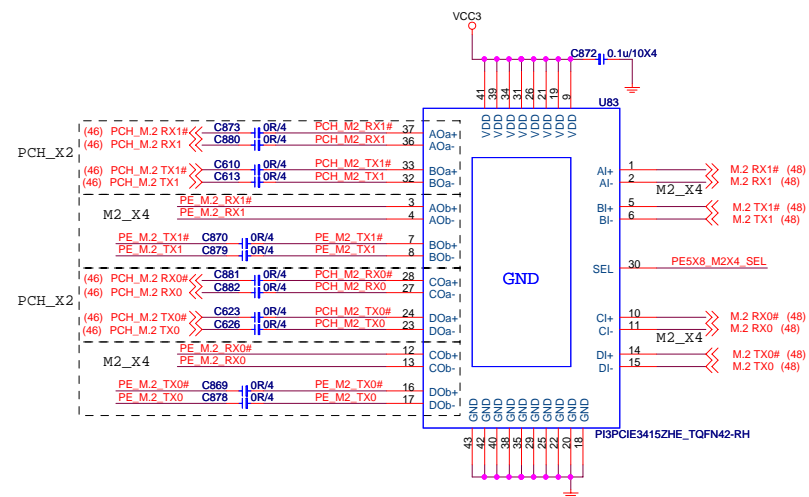
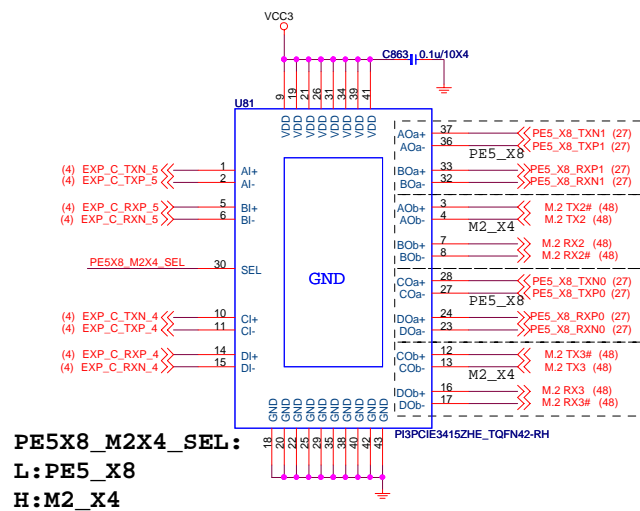
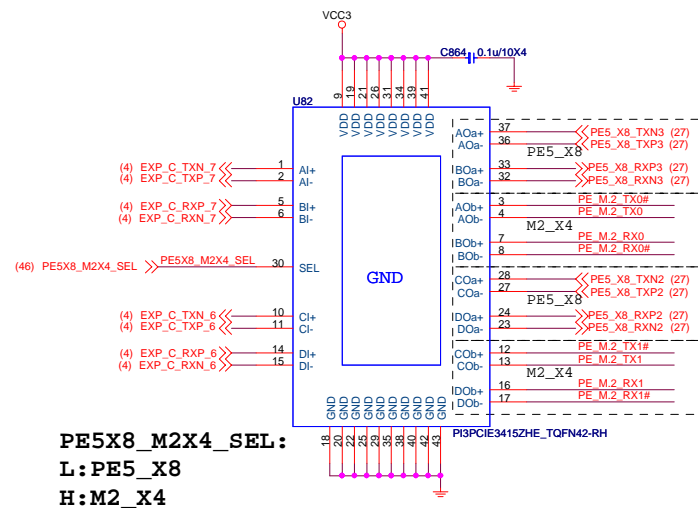
SATA5_6_7_8

Pin	Signal	Function
1	SATA TX4+	R159 0R/4 SETX_0P S2
2	SATA TX4-	R243 0R/4 SETX_0N S2
3	SATA RX4+	R641 0R/4 SERX_0P S6
4	SATA RX4-	R639 0R/4 SERX_0N S6
5	SATA TX5+	R1058 0R/4 SETX_1P S9
6	SATA TX5-	R1057 0R/4 SETX_1N S10
7	SATA RX5+	R1060 0R/4 SERX_1P S13
8	SATA RX5-	R1059 0R/4 SERX_1N S12
9	PETP0/A2+	PETP0/A0-
10	PETP2/A2+	PETN2/A2-
11	PERP0/B0+	PERN0/B0-
12	PERP2/B2+	PERN2/B2-
13	PETP3/A3+	PETN3/A3-
14	PERP3/B3+	PERN3/B3-
15	S16 ST TX6	C567 0.01u16X4
16	S17 ST TX#6	C568 0.01u16X4
17	S20 ST RX6	C596 0.01u16X4
18	S19 ST RX#6	C592 0.01u16X4
19	S23 ST TX7	C573 0.01u16X4
20	S24 ST TX#7	C577 0.01u16X4
21	S27 ST RX7	C586 0.01u16X4
22	S26 ST RX#7	C585 0.01u16X4
23	SATA_TX16	(17)
24	SATA_TX#6	(17)
25	SATA_RX6	(17)
26	SATA_RX#6	(17)
27	SATA_TX7	(17)
28	SATA_TX#7	(17)
29	SATA_RX7	(17)
30	SATA_RX#7	(17)

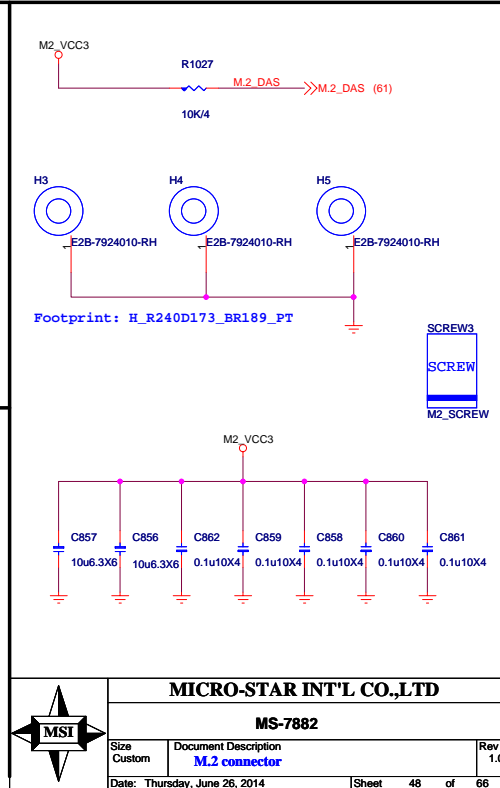
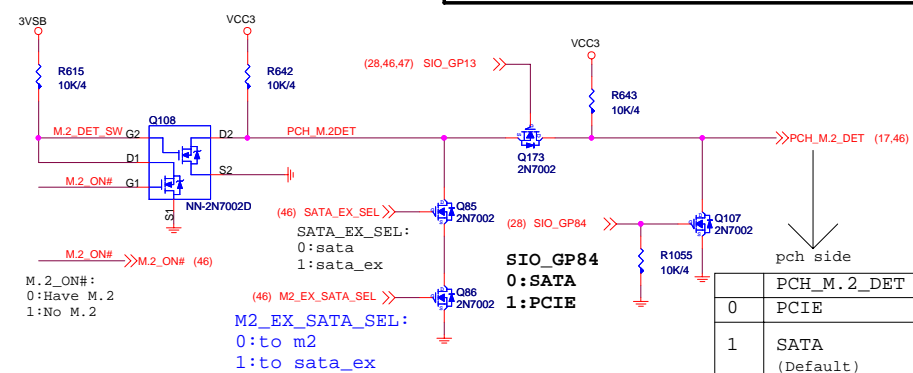
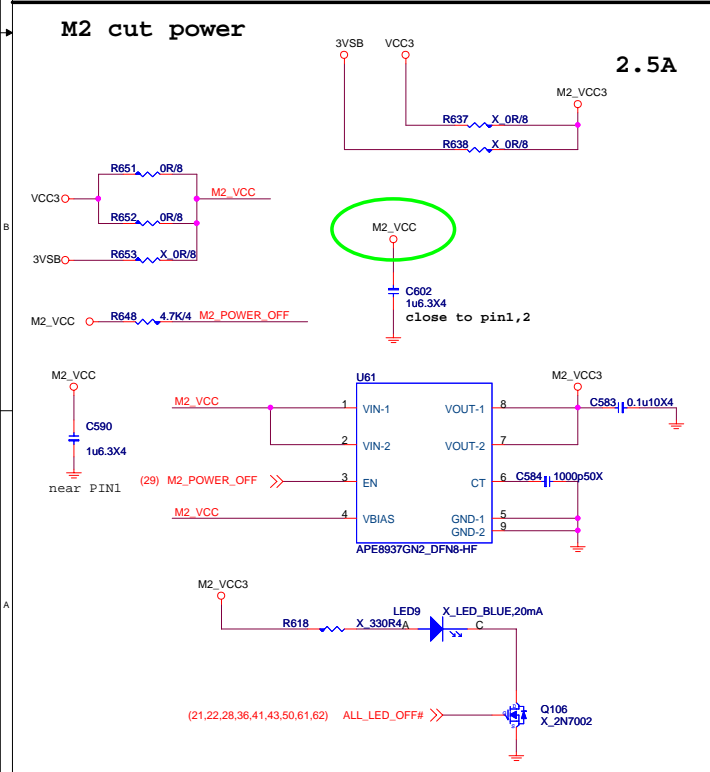
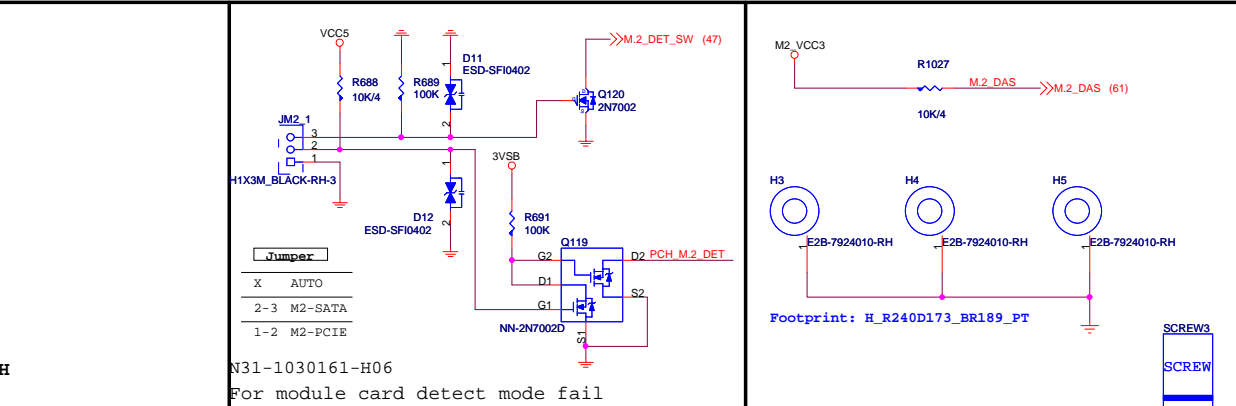
[illegible]

Size Custom	Document Description SATA Connector & Re-driver	Rev 1.0
Date: Thursday, June 26, 2014		Sheet 46 of 66

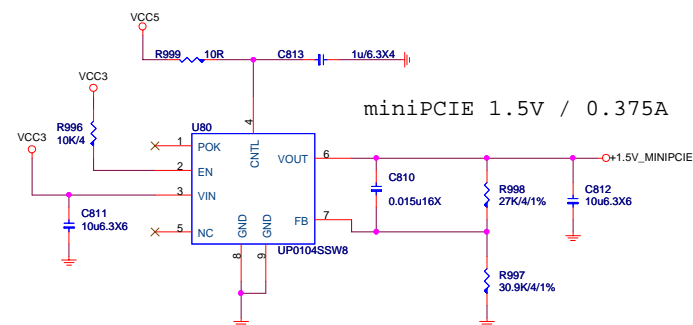
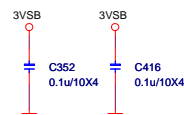
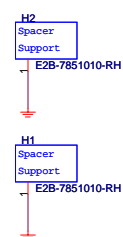
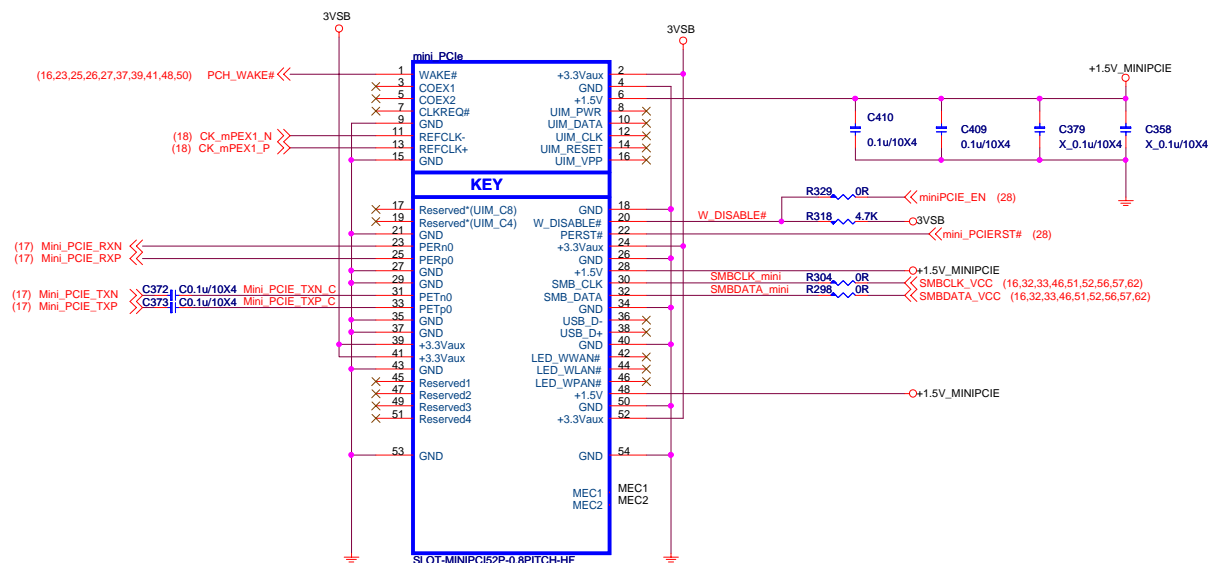
PCIE5 & M.2 Switch



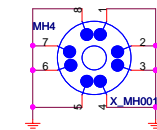
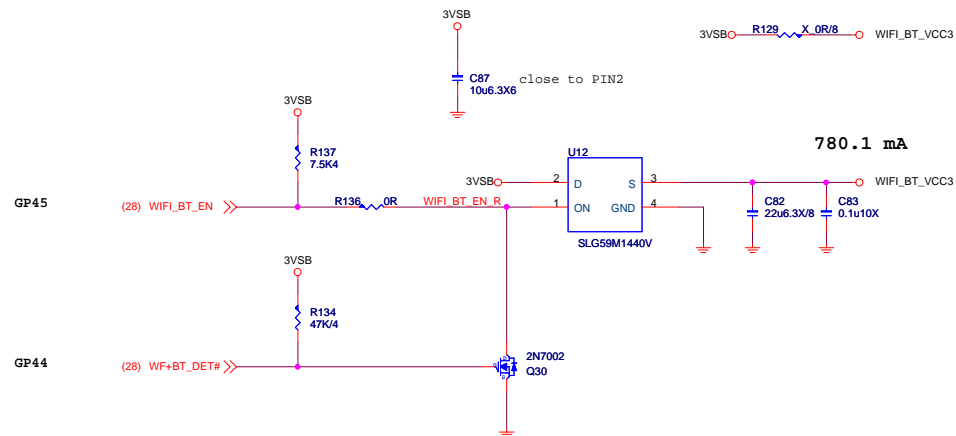
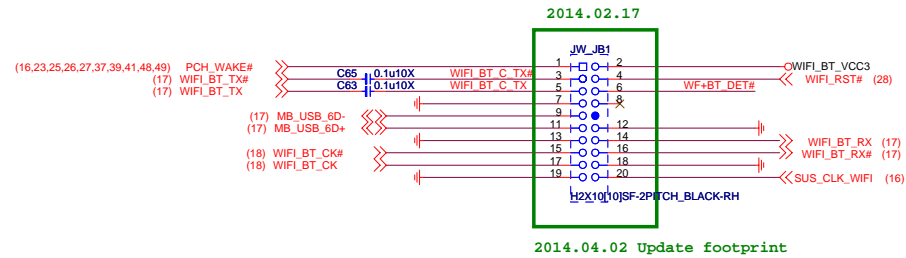
SIO_GP10	SIO_GP80	SIO_GP84	SIO_GP13	Mode
1	0	1:PCIE 0:SATA	0	M2-PCH
X	1	X	0	PCIEX8
X	0	X	0	M2-X4
0	X	1:PCIE 0:SATA	X	SATA Express
GPI(:0)	GPI(:0)	GPI(:0)	1	AUTO



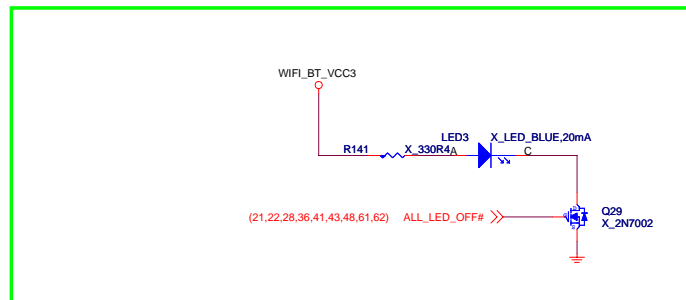
mini PCIE



WIFI + Buletooth



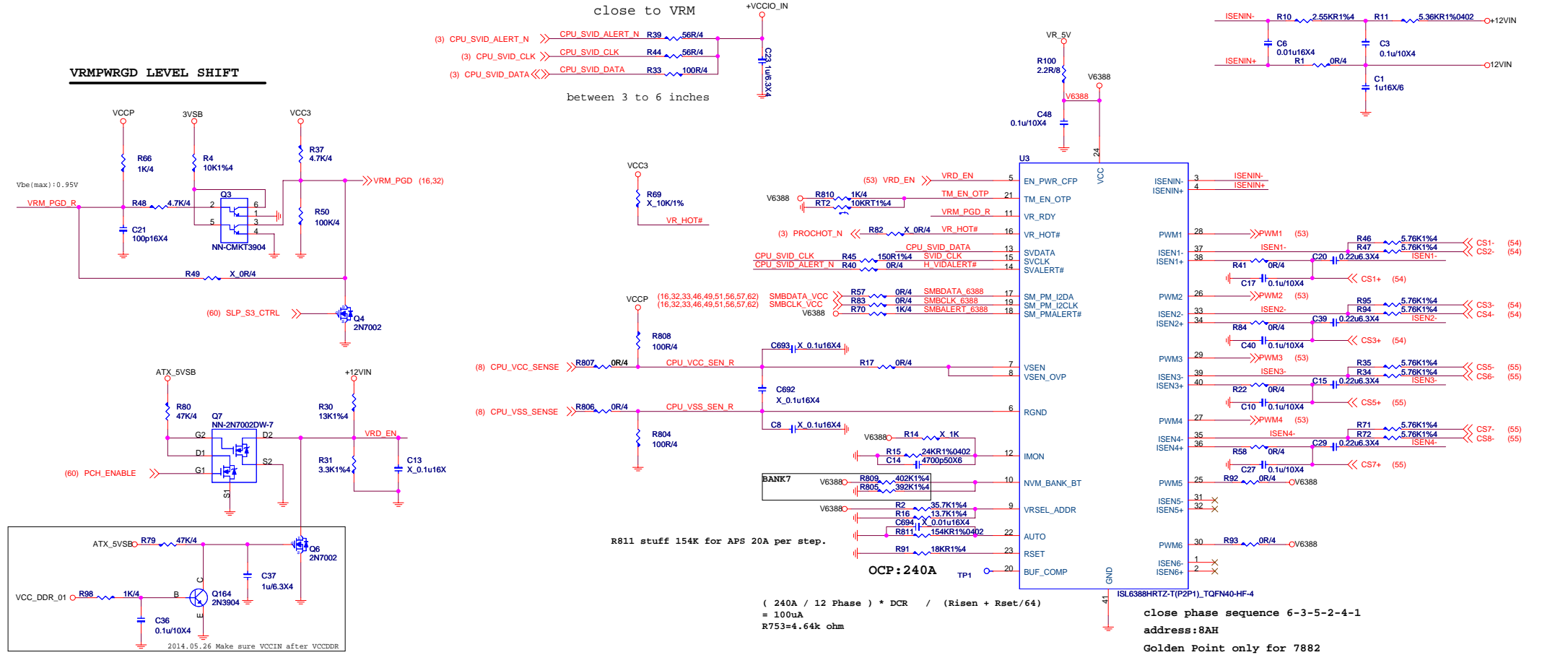
2014.04.02 Update footprint



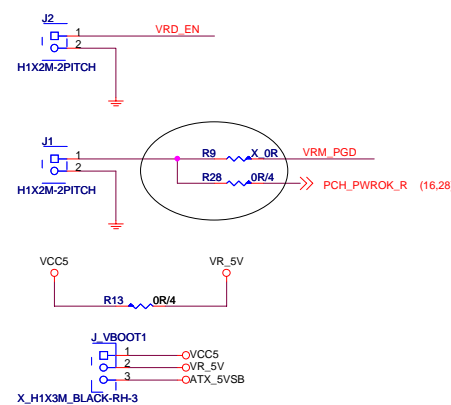
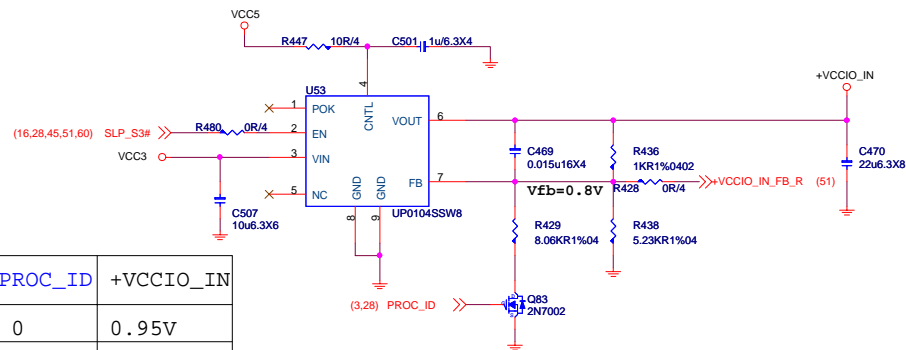
CPU Power-ISL6388-8Phase

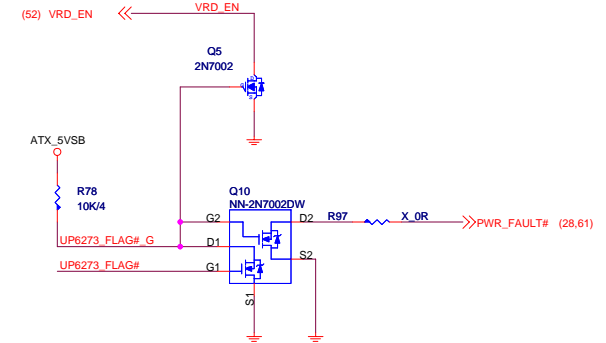
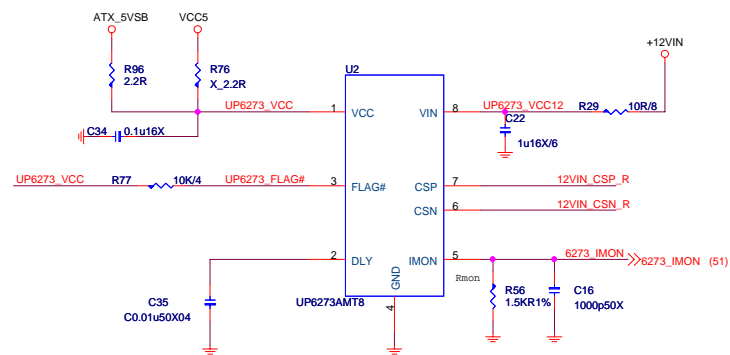
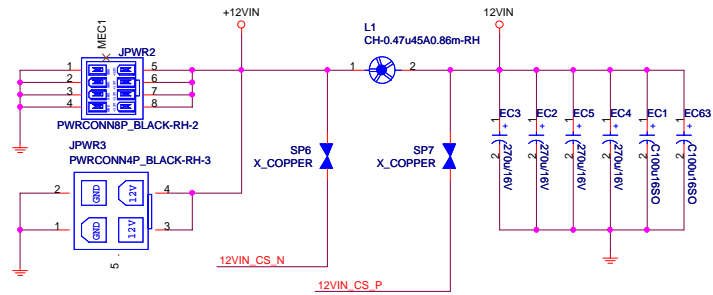
VCCP_1.8V 180A, OC margin 2.5V=240A

OCP:336A for 8Phase



VCCIO_IN_1.05V 431mA, OC margin 1.6V=1A



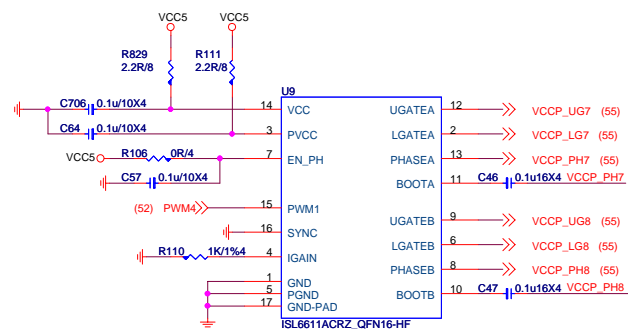
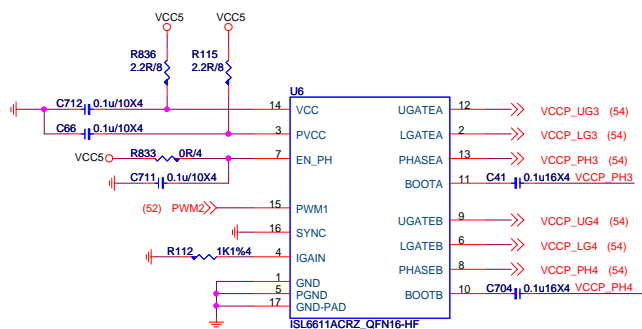
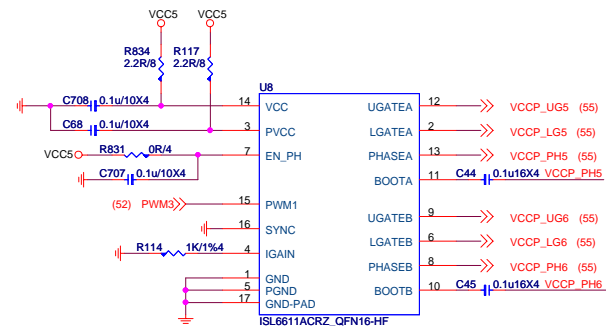
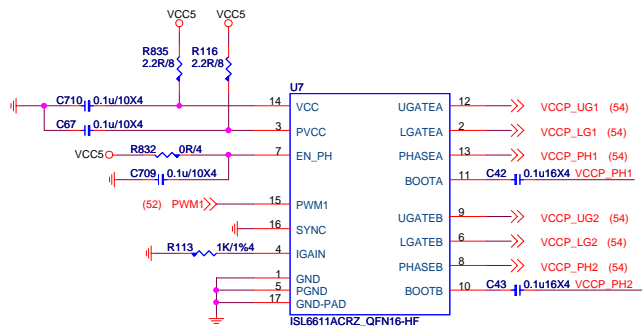
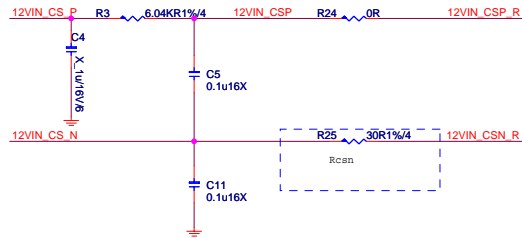


$$I_{in} = (V_{mon} * R_{csn}) / (R_{mon} * R_{dc})$$

$$V_{mon} = 1.2$$

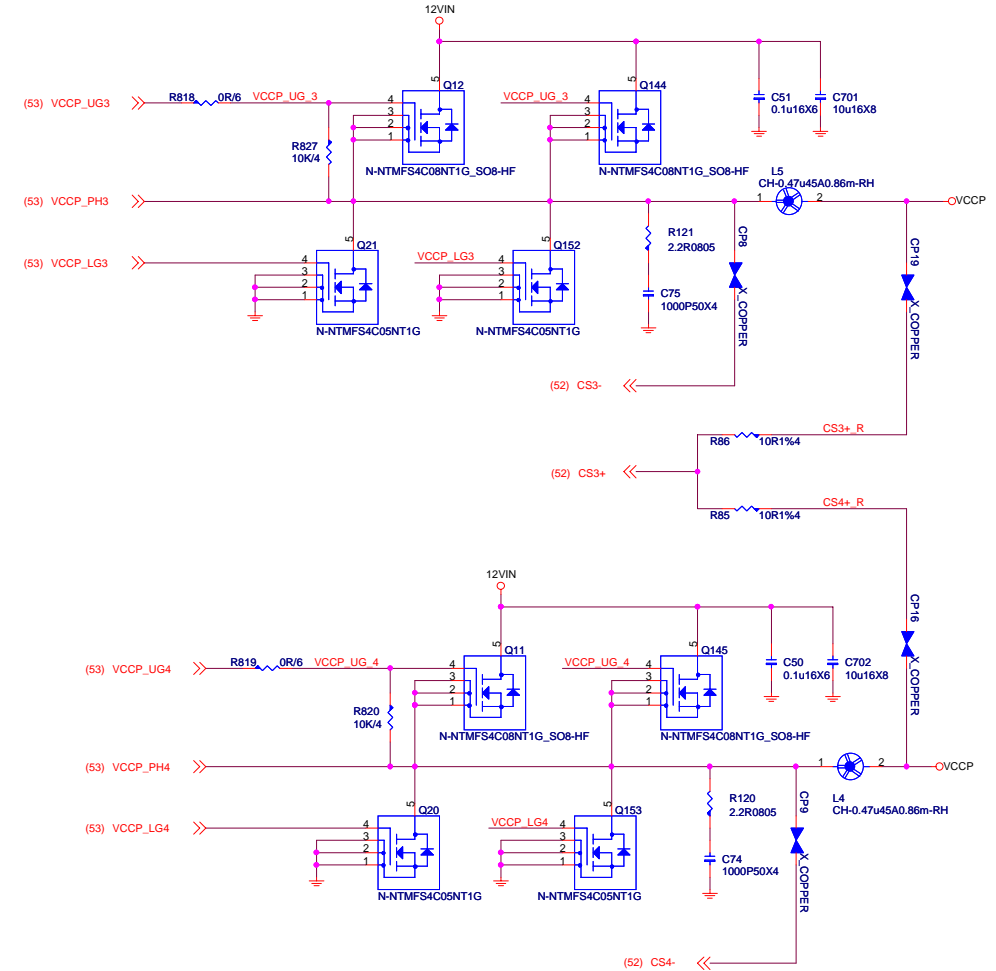
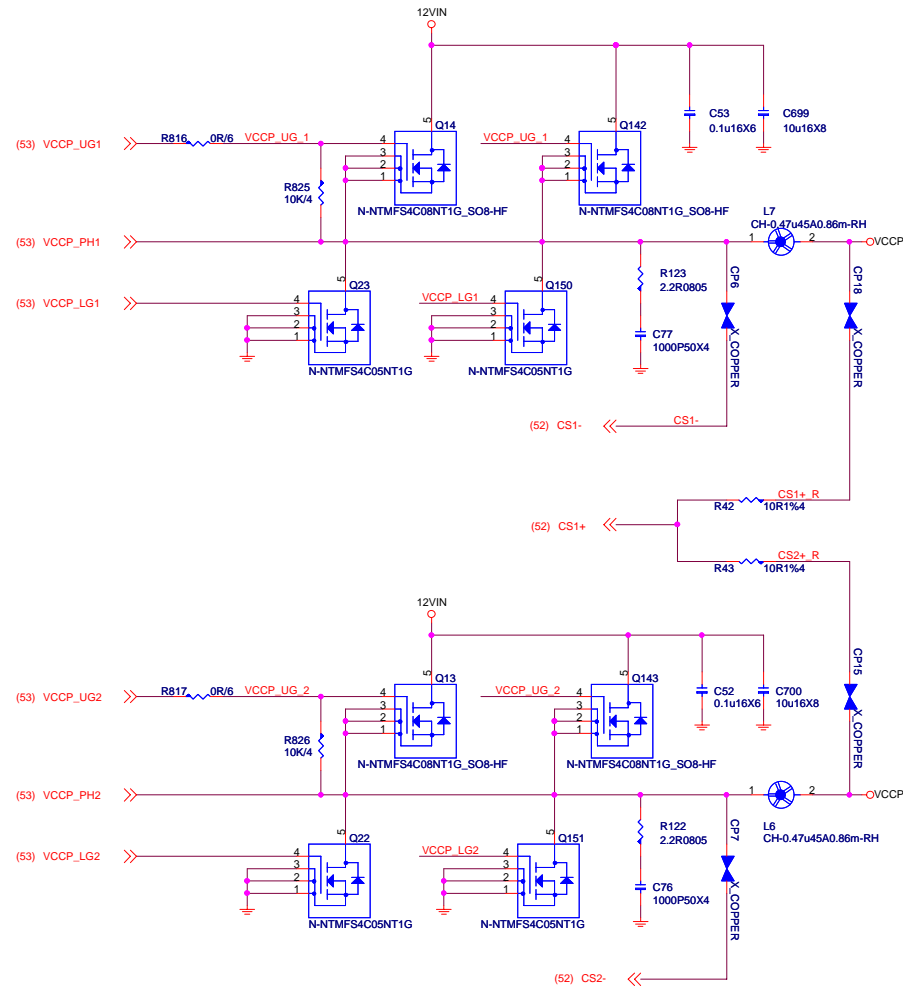
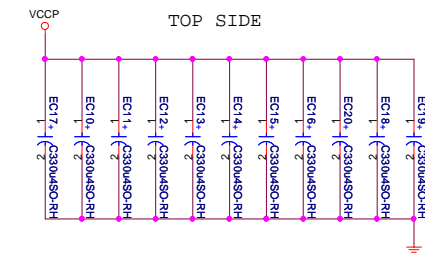
can change OCP trigger level by Rcsn and Rmon

$$(1.2 * 0.2) / (10K * 0.3m) = 80A$$



$$I_{rms} = I_{out} \sqrt{D/N - (D)^2} = 320 \sqrt{0.02 - (0.16)^2} = 23.94A$$

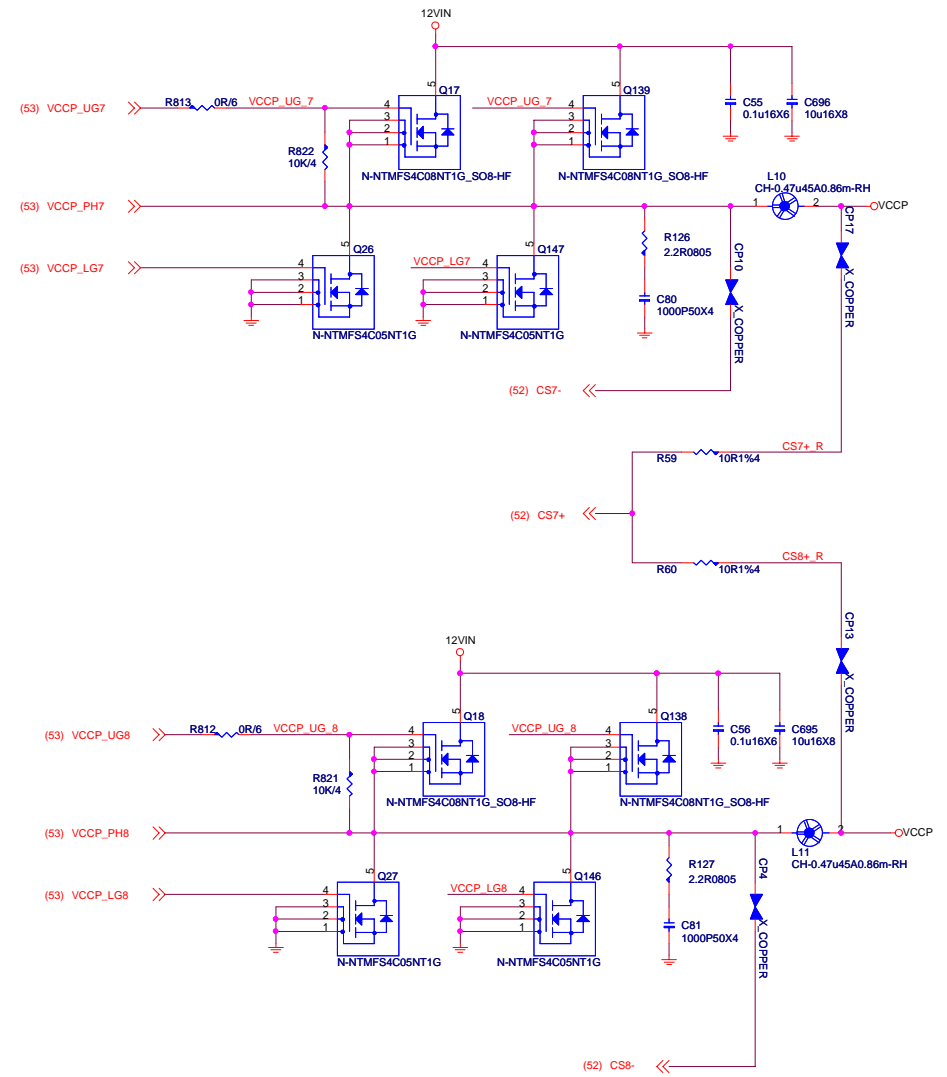
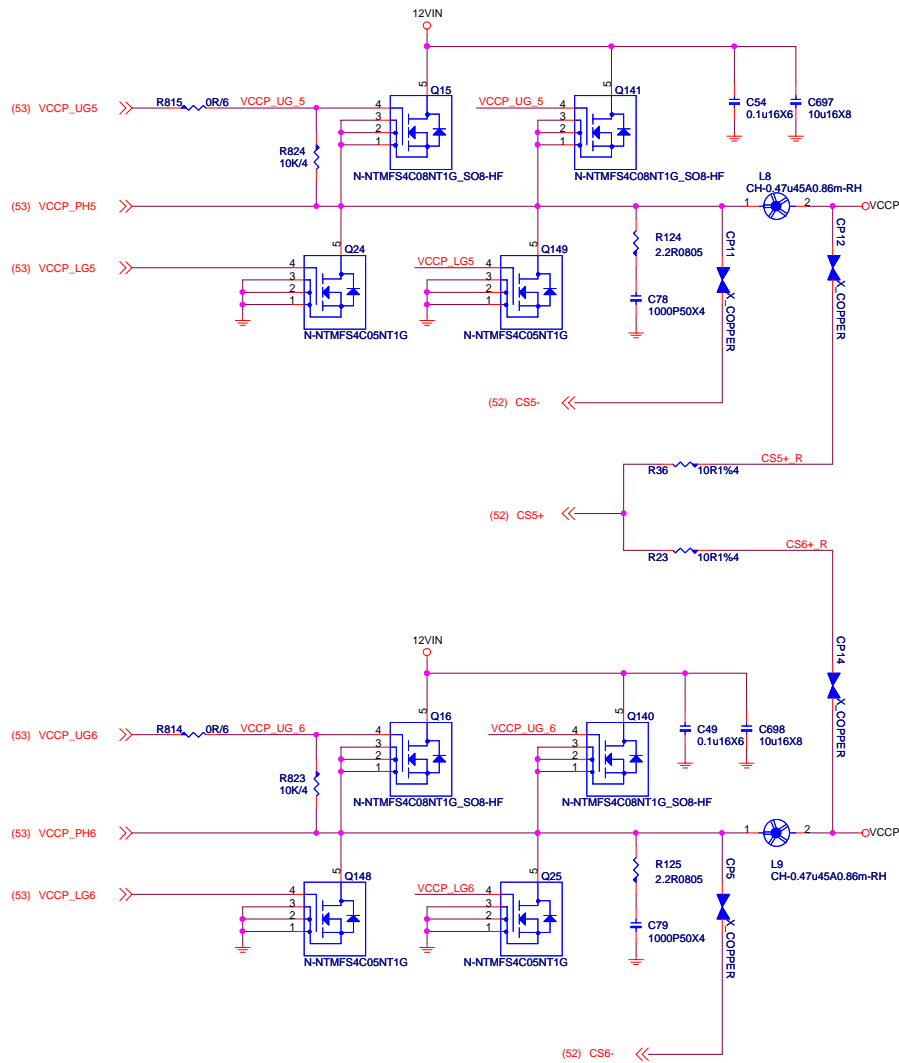
$$5000mA * 5 = 25A > 23.94A$$



MICRO-STAR INT'L CO.,LTD

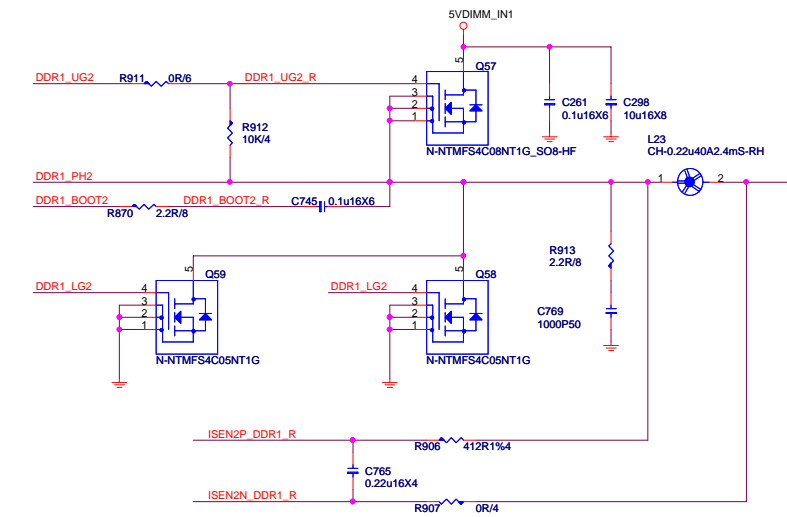
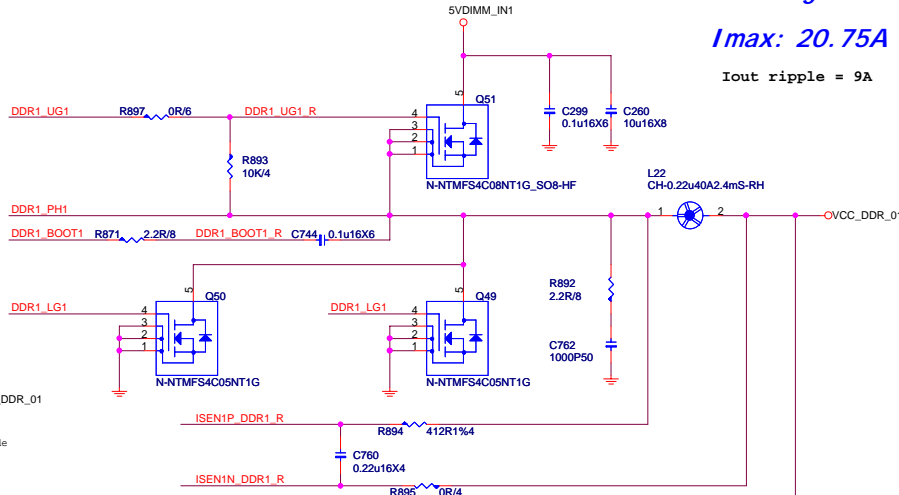
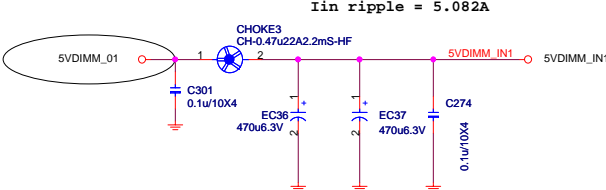
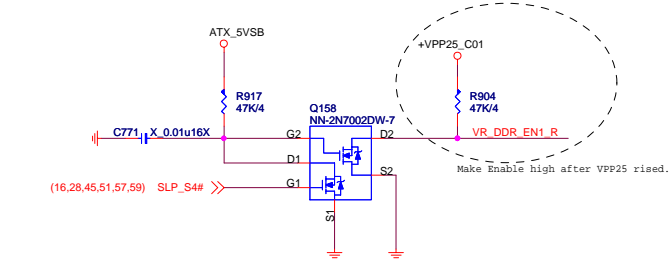
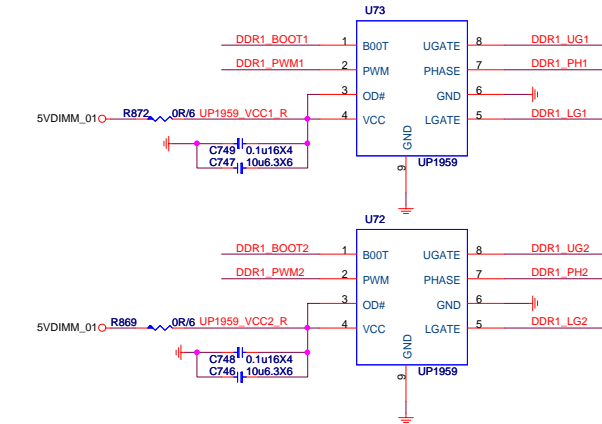
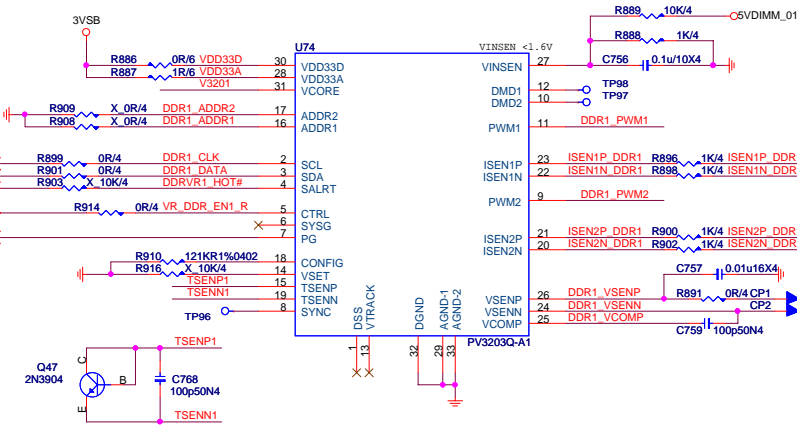
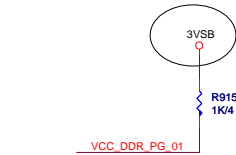
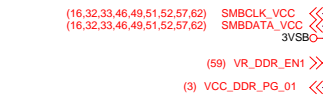
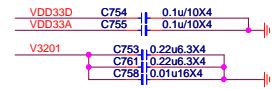
MS-7882

Size Custom	Document Description CPU Power -MOS 1-4	Rev 1.0
Date: Thursday, June 26, 2014	Sheet 54	of 66



DDR Power1-PV3203-2-Phase

DDR4_1.2V 11A, OC margin=44A
OCP:66A for 2Phase



OCP=64A
OC margin=44A
I_{max}: 20.75A
I_{out} ripple = 9A

DDR Power1-PV3203-2-Phase

DDR4_1.2V 11A, OC margin=44A
OCP:66A for 2Phase

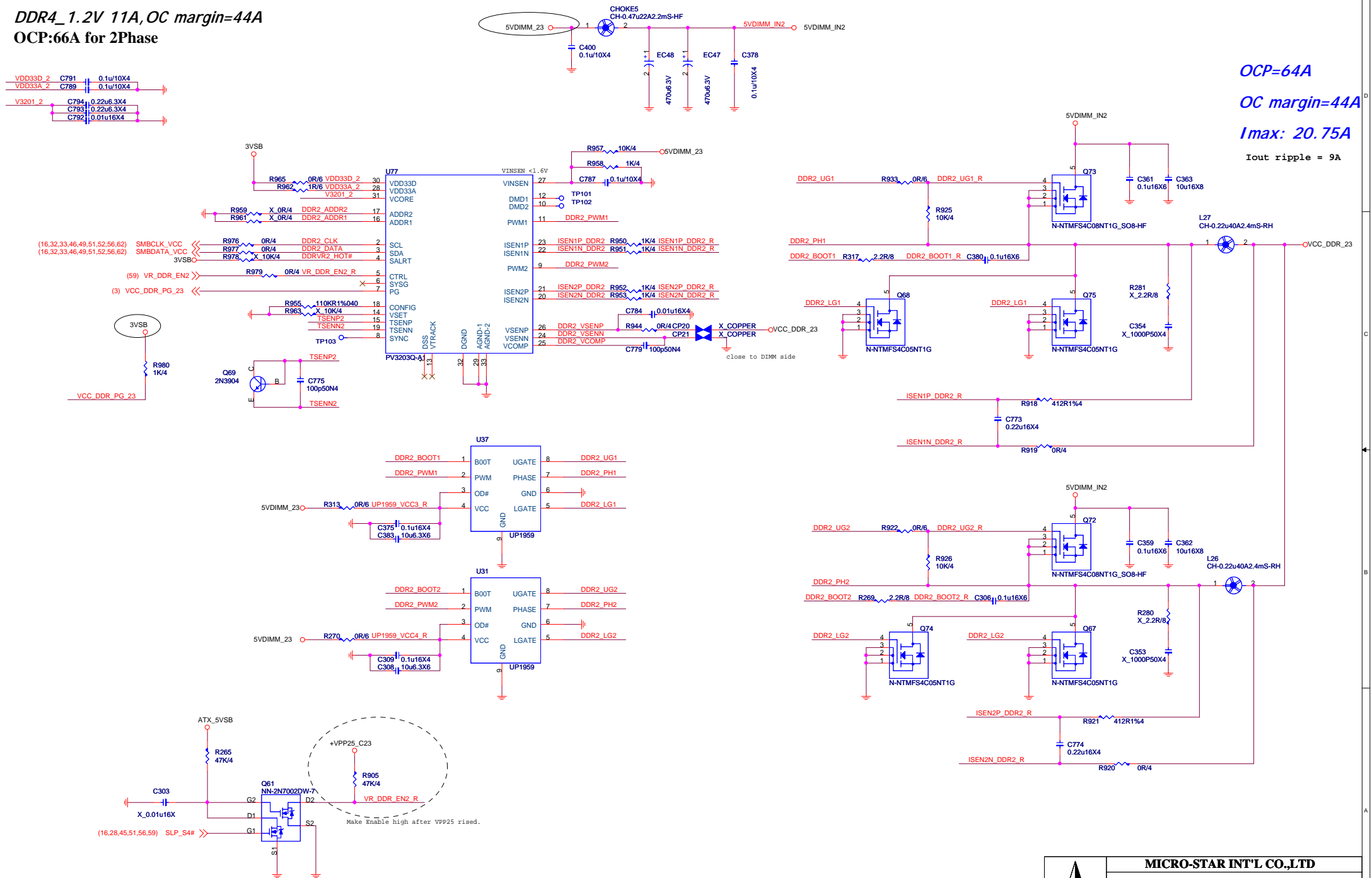
Iin ripple = 5.082A

OCP=64A

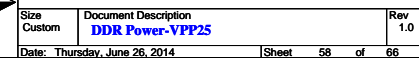
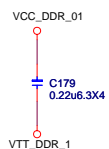
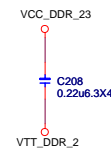
OC margin=44A

I_{max}: 20.75A

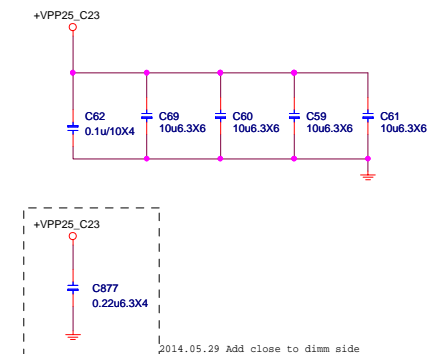
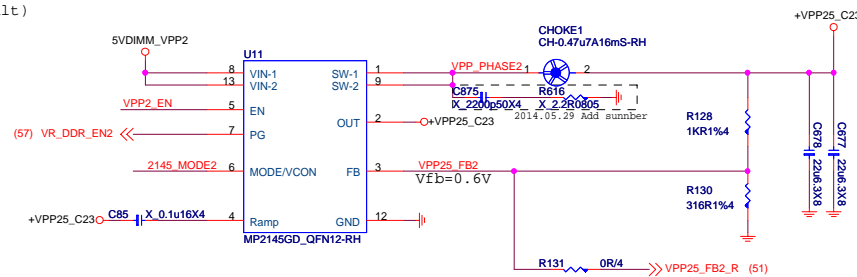
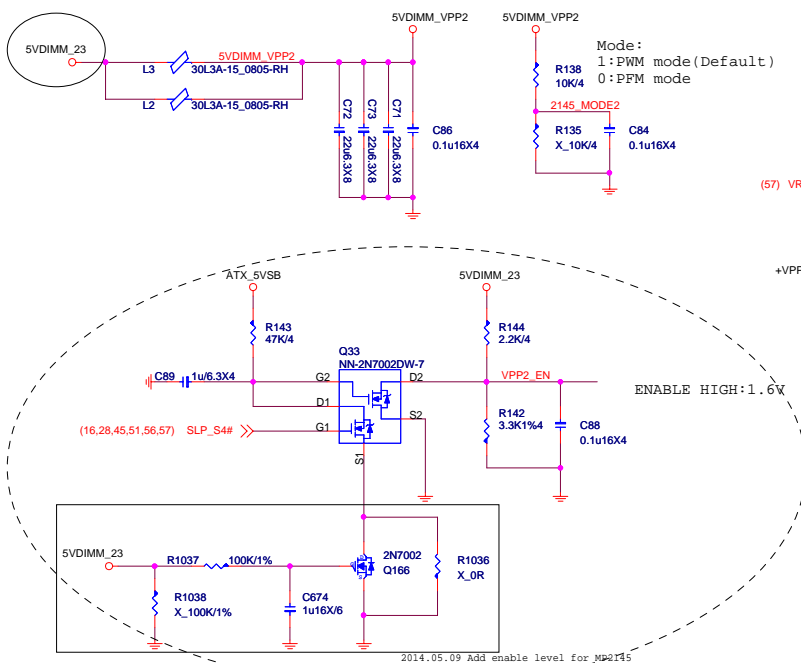
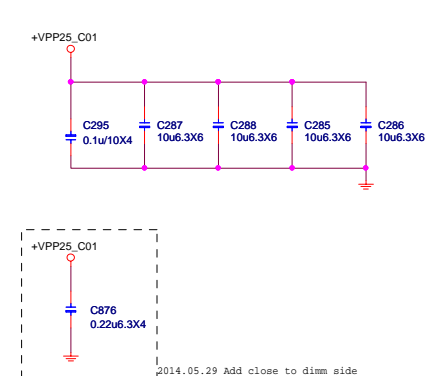
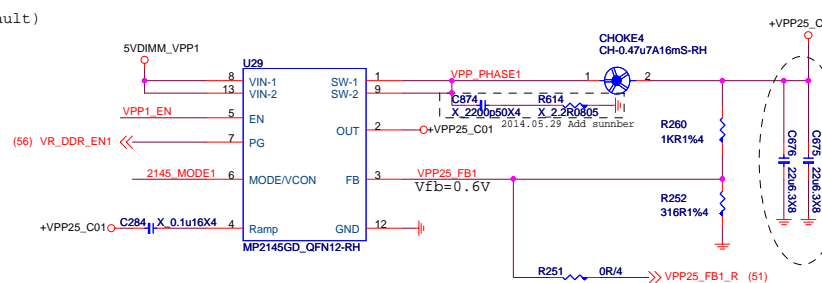
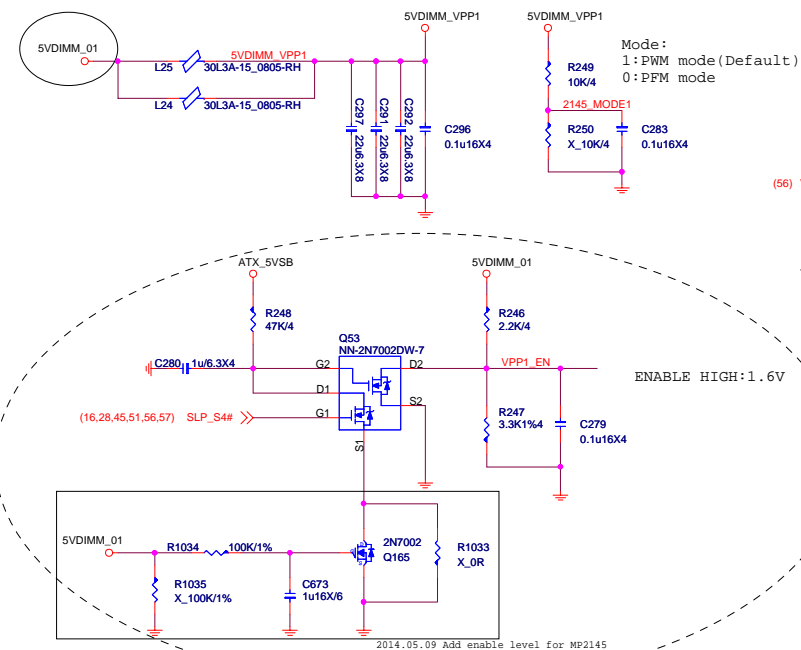
I_{out} ripple = 9A



4DIMM :3A FOR OC margin



4DIMM :6A FOR DDR VPP



MICRO-STAR INT'L CO.,LTD

MS-7882

Size
Custom

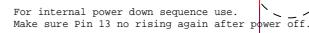
Document Description
DDR Power-VPP25

Rev	1.0
-----	-----

Date: Thursday, June 26, 2014

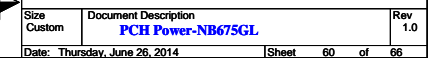
Sheet 59 of 66

OCP calculate:
 $(20\text{mA} * R_{\text{ocs}}) / 4 * R_{\text{ds-on}} = \text{IOCP}$
 $(20\text{mA} * 12.1\text{K}) / 4 * 4\text{mohm} = 15.5\text{A}$

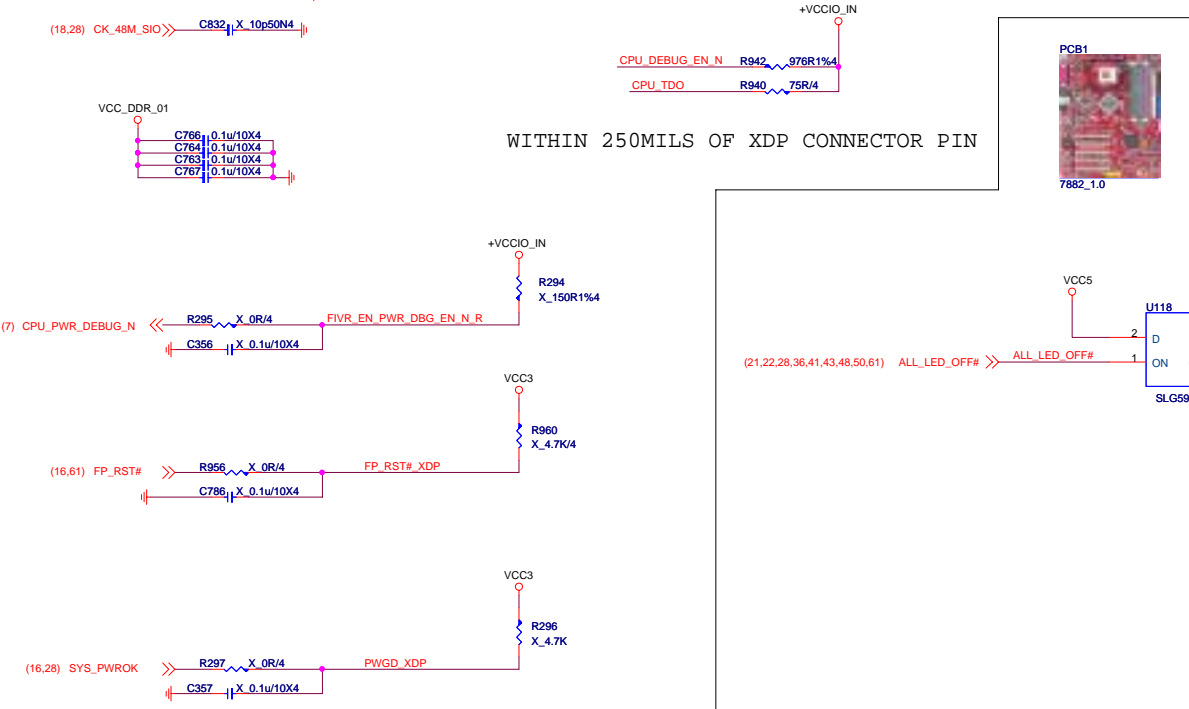
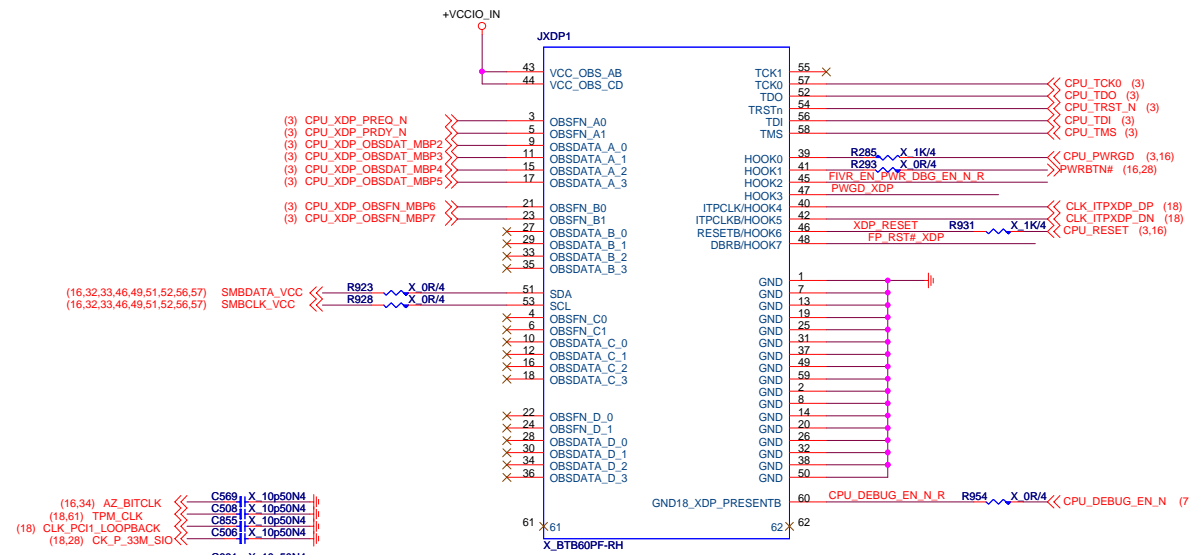


6A

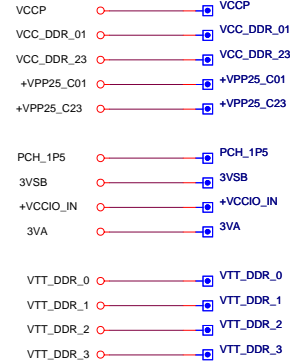
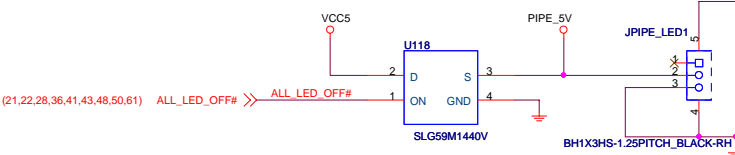
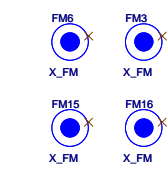
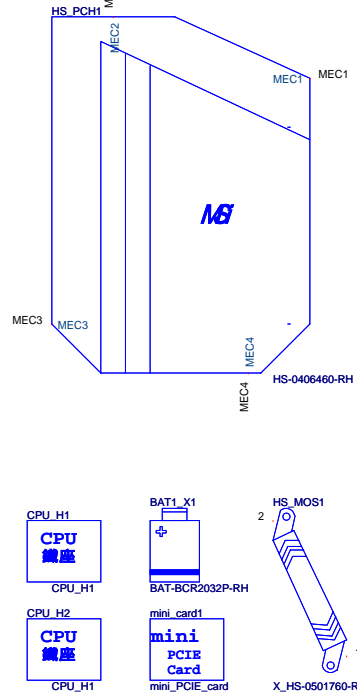
C854 close to PCH



Reserve debug port 5020



WITHIN 250MILS OF XDP CONNECTOR PIN



Mounting Holes

